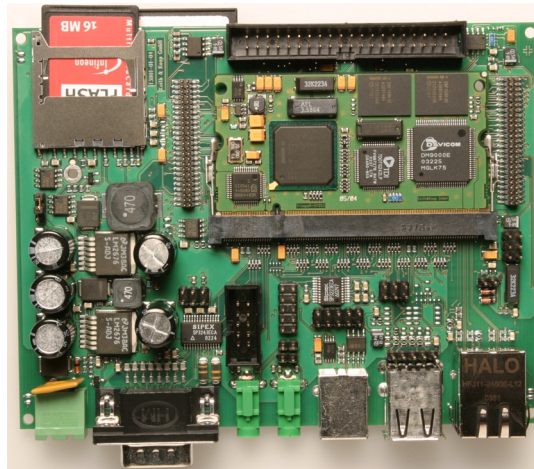


# ConXS

## Documentation 1.1 (preliminary)



## 1.0 Introduction

The ConXS is an industrial terminal based on the Keith & Koep “Trizeps III<sup>1</sup>“ module.

The board offers the following features:

- Ethernet: 10 / 100 MBit RJ45
- Compact Flash Socket Type II
- SD/MMC Card connector
- USB: e.g. 2 x USB host or 1 x USB host and 1 x OTG
- USB slave via PXA255
- Serial via DB9 male
- Serial via 10-pin, or Bluetooth module
- Serial via extension bus for IrDA or custom application
- Externally battery buffered Real Time Clock (RTC)
- Uninterruptible Power Supply interface (optional)
- NV-SRAM (optional)
- Headphone stereo out, Microphone-in mono
- 12V single supply (wide range input)
- Universal LCD connector from sub 1/4 VGA to 16bpp TFT SVGA, LVDS or DVI extensions available

1. Keith & Koep GmbH offers Trizeps III modules based on the Intel XScale PXA255 Microprocessor. The processor works very fast (480 Dhrystone 2.1 MIPS @ 400MHz) and need very low power. The Trizeps III module includes the Philips UCB 1400 (a single chip, integrated mixed signal audio and telecom codec with integrated analog to digital converter and touch screen interface), an Ethernet Controller 100/10 MBit with 32 Bit Businterface, an USB 2.0 OTG controller, a parameter EEPROM. The Trizeps offers up to 64MByte Flash memory and up to 128MByte SDRAM. **(for more details download our Trizeps III documentation)**

- Contrast EEPOT
- Backlight switch
- Hilscher COM-Module connector
- Extension-bus routed through high density CPLD

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## 2.0 Preface

---

### 2.1 Getting started

The ConXS board is designed as a motherboard for Trizeps III. The first part of this chapter gives a physical description of the board and the second part describes:

1. How to unpack the board and how to make a visual inspection.
2. How to power up the board for the first time.
3. How to connect the board to a host system

#### 2.1.1 Physical description

The physical layout of the board is shown in figure 6 on page 21 (You'll find details on the last page). The dimensions of the board are 130 x 100 mm (LxW). You can find all measures at figure 8 on page 44 and at figure 9 on page 45.

There are a number of header blocks on the board that accept 2-pin jumpers, allowing the board to be configured in different ways. Due to further header blocks it is possible to connect an LCD-display with touch screen. A serial connection to a host system is possible by using one of the RS232 interfaces.

#### 2.1.2 Unpacking the board

The ConXS contains electronic components that are susceptible to electrostatic discharge (static electricity). To avoid electrostatic damage the board is supplied in an antistatic bag. When handling the card, risk of damage can be diminished by taking a few simple precautions:

1. Do not remove the card from the bag unless you are working on an antistatic, grounded surface and wearing an grounded antistatic wrist strap.
2. Keep the antistatic bag the card was supplied in; if you remove the card from a system, store it in the bag.

Normally ConXS is supplied with a Trizeps III in the SODIMM-socket. If the SODIMM is not fitted with Trizeps III when you receive your board, follow the next instructions:

1. Slide the Trizeps III into the socket taking account of the polarity mark. Do not touch the gold contacts. You can see that there is a polarization mark cut in the Trizeps III; this ensures that the Trizeps III is adjusted correctly. Put the Trizeps III modul carefully at an angle of about 30 degrees into the socket.
2. Support the underside of the board and push the Trizeps III down into the socket. It should click into its place with a gentle click.

Before you install and power up your ConXS, you should perform a short visual inspection:

1. Inspect the card for physical damage.

2. Ensure that each of the 2-pin jumpers is pushed down firmly onto its mounting posts. If you move any of the jumpers, refer to Appendix A to ensure they are replaced correctly.

#### 2.1.3 Powering up the first time

Use Appendix A to ensure the jumpers are set appropriately. If you need more details on how to install the card or attach power supply, refer to Appendix A, too.

#### 2.1.4 How to connect the board to host system

Use an RS232 null-modem cable to attach the serial interface on the board to an RS232 port on a terminal or terminal emulator. For example, you could connect it to a PC running Windows and use the Windows Terminal or Hyperterminal application. Configure the terminal to operate at 38 kbaud, 8-bit data, 1 stop bit, no parity, no flow control. If you need more details on choosing an appropriate cable, refer to appendix A.

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### 3.0 Functional specification

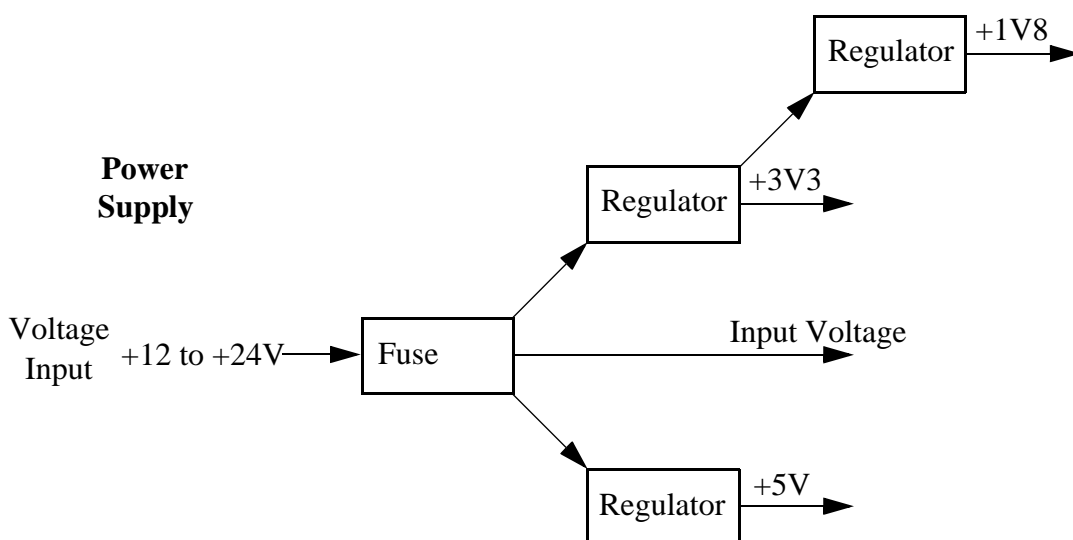
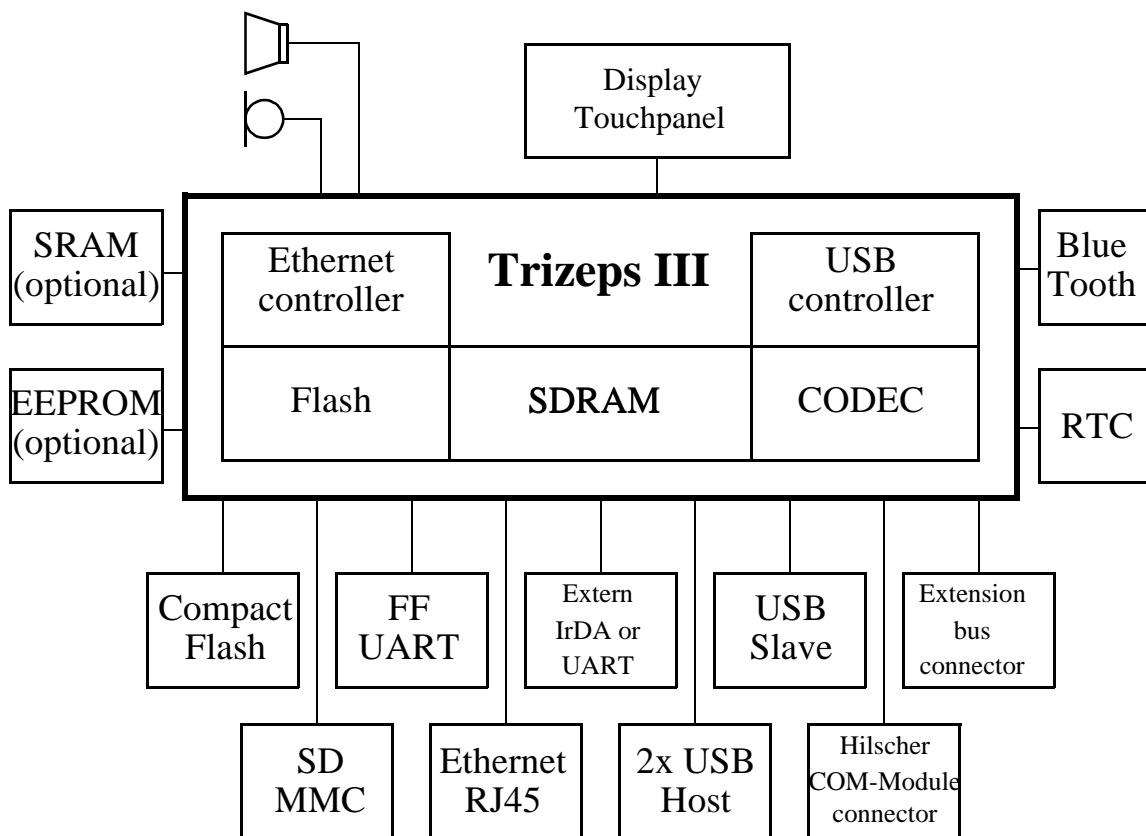
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This chapter describes each functional element on the ConXS board. In the next chapters you can find more detailed information about the board and some important hints for programming it. The block diagram on figure 1 on page 4 shows the interconnections of the major elements.

#### Components of ConXS:

1. Trizeps III module
2. Serial EEPROM (optional)
3. Compact Flash socket type II
4. Board Control Register BCR
5. Real Time Clock
6. Reset
7. Power Supply
8. Power generation on board
9. GPIO
10. Ethernet
11. UART serial ports
12. TTL I/O
13. Audio in/out
14. Display connector, 4 wire Touch Panel, contrast EEPROM and backlight switch
15. SD / MMC connector
16. Powerfail - Interrupt
17. Uninterruptible Power Supply (UPS)
18. USB host
19. NV-SRAM
20. Contrast EEPROM
21. Backlight switch
22. Hilscher COM-Module connector
23. Extension bus

FIGURE 1. ConXS block diagram



### 3.1 Trizeps III module

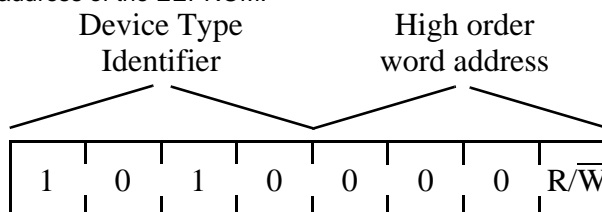
The Trizeps III Module is based on the Intel® XScale™ core-based CPU (200, 300 and 400 MHz) PXA255 - ARM Architecture v.5TE compliant and application code compatible with Intel® SA-1110 processor which is used on the Trizeps I module. The CPU based on Intel® Superpipelined RISC technology utilizing advanced Intel 0.18μ process for high core speeds at low power (480K Dhrystone 2.1 per second @ 400 MHz). Some features of the XScale: Integrated memory and PCMCIA/CompactFlash Controller with 100MHz Memory Bus, 16-bit or 32-bit ROM/Flash/SRAM six banks, 16-bit or 32-bit SDRAM; System Control Module includes 17 dedicated general-purpose interruptible I/O ports, real-time clock, watchdog and interval timers, power management controller, interrupt and reset controller, LCD controller and two on-chip oscillators. Trizeps-III includes also the Philips UCB 1400, on a single chip it combines audio codec functions, a touch-screen controller and power management interfaces. The incorporated A/D converter and the touch screen interface provides complete control and read-out of a 4 wire resistive touch screen. Furthermore the Trizeps III module has an Ethernet controller (DM9000 by Davicom, 10/100 MBit) and an USB Host controller (OTG242 by Transdimension).

### 3.2 Serial EEPROM (optional)

ConXS provides a serial EEPROM (X24C16- Xicor) to be used as a non-volatile memory. It has a size of 16KBit and it is internal organized as 2048 x 8. The X24C16 offers a serial interface and a software protocol allowing operation on a simple two wire bus with I<sup>2</sup>C\_CLK (SCL of PXA255) and I<sup>2</sup>C\_DATA (SDA of PXA255). The EEPROM is optional and usually not placed.

FIGURE 2.

The slave address of the EEPROM:



- Read address: A1
- Write address: A0

### 3.3 CompactFlash socket type II

CompactFlash is a very small removable mass storage device. It provides complete PCMCIA-ATA functionality and compatibility plus TrueIDE functionality compatible with ATA/ATAPI-4. At 43mm (1.7“) x 36mm (1.4“) x 3.3mm (0.13“), the device's thickness is less than one-half of a current PCMCIA Type II card. It is actually one-fourth the volume of a PCMCIA card. Compared to a 68-pin PCMCIA card, a CompactFlash card has 50 pins (the connector is similar to the PCMCIA card) but still conforms to PCMCIA-ATA specs. CompactFlash cards are designed with flash technology, a non-volatile storage solution that does not require a battery to retain data indefinitely. CompactFlash storage products are solid state, meaning they contain no moving parts, and provide users with much greater protection of their data than conventional magnetic disk drives.

The ConXS is delivered with a Type II CompactFlash socket.

**TABLE 1.** CF Status Register

Offset 0x00000000															CF Status Register			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Reserved												VS[1:0]		BVD[1:0]				
Bits	Name		Type	Description														
1:0	BVD[2..1]		Read Only	Charge Condition of PC-card 00 - Battery low, data loss 01 - Warning, battery must be changed, but no data loss till now 10 - Battery low, data loss 11 - Battery OK														
3:2	VS[2:1]		Read Only	Voltage Sense lines 11 - 5V operation (unsupported) 0x - 3V3 operation														

### 3.4 Board Control Register BCR

The ConXS board requires additional GPIO output functions, which are implemented in the Board Control Register (BCR) to control the Compact Flash, display and something else.

**TABLE 2.** Board Control Register

Offset 0x02000000															Board Control Register			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Reset	?	?	?	?	?	?	?	?	0	0	1	0	0	0	0	0		
Reserved										CF_RESET	Reserved	CF_BUF_EN	L_DISP	Reserved	Reserved	S0_POW_EN [0..1]		
Bits	Name		Type	Description														
1:0	S0_POW_EN[1..0]		Write Only	CompactFlash Power Enable x1, 1x - Power ON 00 - Power OFF														
2	Reserved		-	-														
3	Reserved		-	-														

TABLE 2.

Board Control Register

Offset 0x02000000									Board Control Register							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	?	?	?	?	?	?	?	?	0	0	1	0	0	0	0	0
	Reserved								CF_RESET	Reserved	CF_BUF_EN	L_DISP	Reserved	Reserved	S0_POW_EN [0..1]	
	4	L_DISP		Write Only		Display enable 0 - Display off 1 - Display on										
	5	CF_BUF_EN		Write Only		Compact Flash buffer enable 0 - CF buffer enable ON 1 - CF buffer enable OFF										
	6	Reserved		-		-										
	7	CF_RESET		Write Only		Resetting Compact Flash card 0 - Normal operation 1 - Resetting PCMCIA										

With setting the data bus D04 the display control signal L\_DISP can be switched. The important thing about that is the power on/off timing of the display. Usually the correct sequence is as followed:

1. Power Supply
2. Input signal
3. Contrast voltage
4. Display control signal L\_DISP

If you use another display as delivered from Keith & Koep you should test the correctness of the power on/off sequences.

Resetting the data bus D05 switches the address and control-signals of the CF-buffer.

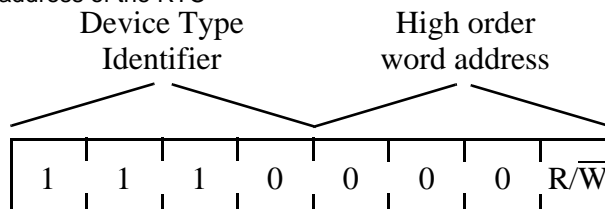
With setting the data bus D07 a reset-signal is sent to the Compact Flash slot.

### 3.5 Real Time Clock (RTC)

ConXS contains a Low-Power RTC from Philips, called PCF8593. This chip uses the same two wire bus as the serial EEPROM, which is described in figure 2 on page 5.

FIGURE 3.

The slave address of the RTC



Read address: A3

Write address: A2

The RTC is supplied from an external battery.

### 3.6 Reset

There are two sources of reset on the ConXS:

1. Power-on Reset
2. Reset from the watchdog timer

Power-on reset is generated automatically when power is applied to the board. It can also be initiated by a push button switch attached to a 2-pole 0.1-inch pitch connector on the board.

Resets generated by any of these methods are equivalent and indistinguishable.

### 3.7 Power Supply

The power supply is done through a 2-pin connector by Phoenix. The input voltage range is between +12V and +24V.

### 3.8 Power generation on board

The power supplies +5V and +3V3 are generated from the input voltage by two DC-DC converters. The +5V are used by USB or CompactFlash cards and for back-light inverter. The +3V3 are used by Trizeps III, CompactFlash cards, serial interfaces and something else. The +1V8V is generated from +3V3, it is needed as core voltage of the CPLD.

### 3.9 GPIO

The PXA255 processor enables and controls its 81 general purpose I/O (GPIO) pins through the use of 27 registers which configure the pin direction (input or output), pin function, pin state (outputs only), pin level detection (inputs only), and selection of alternate functions. The PXA255 processor provides 81 GPIO pins for use in generating and capturing application specific input and output signals. Each pin can be programmed as either an input or output. When programmed to be an input, a GPIO can also serve as an interrupt source. If a GPIO is used for its alternate func-

tion it cannot be used as a GPIO at the same time. The table below shows each GPIO pin with the using on ConXS and its corresponding alternate function.

TABLE 3.

GPIOs of PXA255 (Trizeps III) used on ConXS and their alternate functions

PXA255 Pin	Function on ConXS	Dir	Description	Alternate function	Dir
GP[80]	$\overline{\text{CS}}[4]$	out	Active low chip select 4	nCS[4]	out
GP[79]	$\overline{\text{CS}}[3]$	out	Active low chip select 3	nCS[3]	out
GP[78]	internally used on Trizeps III	-	Active low chip select 2	nCS[2]	out
GP[77]	L_BIAS	out	LCD AC BIAS	LCD_ACBIAS	out
GP[76]	L_PCLK	out	LCD pixel clock	LCD_PCLK	out
GP[75]	L_LCLK	out	LCD line clock	LCD_LCLK	out
GP[74]	L_FCLK	out	LCD frame clock	LCD_FCLK	out
GP[73]	LDD15	out	LCD data pin 15	LDD[15]	out
GP[73]			Memory controller grant	MBGNT	out
GP[72]	LDD14	out	LCD data pin 14	LDD[14]	out
GP[72]			32 KHz clock	32 kHz	out
GP[71]	LDD13	out	LCD data pin 13	LDD[13]	out
GP[71]			3.6 MHz oscillator clock	3.6 MHz	out
GP[70]	LDD12	out	LCD data pin 12	LDD[12]	out
GP[70]			Real Time Clock (1Hz)	RTCCLK	out
GP[69]	LDD11	out	LCD data pin 11	LDD[11]	out
GP[69]			MMC_CLK	MMCCLK	out
GP[68]	LDD10	out	LCD data pin 10	LDD[10]	out
GP[68]			MMC Chip Select 1	MMCCS1	out
GP[67]	LDD09	out	LCD data pin 9	LDD[9]	out
GP[67]			MMC Chip Select 0	MMCCS0	out
GP[66]	LDD08	out	LCD data pin 8	LDD[8]	out
GP[66]			MBREQ	MBREQ	in
GP[58]- GP[65]	LDD[00-07]	out	LCD data pin 0 to7	LDD[0-7]	out
GP[57]	$\overline{\text{PIOIS}}16$	in	Bus Width select I/O card	nIOIS16	in
GP[56]	$\overline{\text{PWAIT}}$	in	Wait signal for card space	nPWAIT	in
GP[55]	$\overline{\text{PREG}}$	out	Card address bit 26	nPREG	out
GP[54]	PSKTSEL	out	Socket select for card space	PSKTSEL	out
GP[54]			MMC Clock	MMCCLK	out
GP[53]	$\overline{\text{PCE}}2$	out	Card Enable for card space	nPCE[2]	out
GP[53]			MMC Clock	MMCCLK	out
GP[52]	$\overline{\text{PCE}}1$	out	Card Enable for card space	nPCE[1]	out
GP[51]	$\overline{\text{PIOW}}$	out	I/O Write for Card space	nPIOW	out
GP[50]	$\overline{\text{PIOR}}$	out	I/O Read for Card space	nPIOR	out
GP[49]	$\overline{\text{PWE}}$	out	Write enable for card space	nPWE	out
GP[48]	$\overline{\text{POE}}$	out	Output Enable for card space	nPOE	out

TABLE 3.

GPIOs of PXA255 (Trizeps III) used on ConXS and their alternate functions

PXA255 Pin	Function on ConXS	Dir	Description	Alternate function	Dir
GP[47]	TXD_2	out	STD_UART transmit data	TXD	out
GP[47]			ICP transmit data	ICP_TXD	out
GP[46]	RXD_2	in	STD_UART receive data	RXD	in
GP[46]			ICP receive data	ICP_RXD	in
GP[45]	BT_RTS	out	BTUART request to send	BTRTS	out
GP[44]	BT_CTS	in	BTUART clear to send	BTCTS	in
GP[43]	BT_TXD	out	BTUART transmit data	BTTXD	out
GP[42]	BT_RXD	in	BTUART receive data	BTRXD	in
GP[41]	FF_RTS	out	FFUART request to send	RTS	out
GP[40]	FF_DTR	out	FFUART data terminal ready	DTR	out
GP[39]	FF_TXD	out	FFUART transmit data	FFTXD	out
GP[39]			MMC Chip select 1	MMCCS1	out
GP[38]	FF_RI	in	FFUART ring indicator	RI	in
GP[37]	FF_DSR	in	FFUART data set ready	DSR	in
GP[36]	FF_DCD	in	FFUART data carrier detect	DCD	in
GP[35]	FF_CTS	in	FFUART clear to send	CTS	in
GP[34]	FF_RXD	in	FFUART receive data	FFRXD	in
GP[34]			MMC chip select 0	MMCCS0	out
GP[33]	internally used on Trizeps III	-	Active low chip select 5	nCS[5]	out
GP[32]	GPIO32		AC97 Sdata_in1	SDATA_IN1	in
GP[31]	internally used on Trizeps III	-	AC97 sync	SYNC	out
GP[31]			I2S sync	SYNC	out
GP[30]	internally used on Trizeps III	-	AC97 Sdata_out	SDATA_OUT	out
GP[30]			I2S Sdata_out	SDATA_OUT	out
GP[29]	internally used on Trizeps III	-	AC97 Sdata_in0	SDATA_IN0	in
GP[29]			I2S Sdata_in	SDATA_IN	in
GP[28]	internally used on Trizeps III	-	AC97 bit_clk	BITCLK	in
GP[28]			I2S bit_clk	BITCLK	in
GP[28]			I2S bit_clk	BITCLK	out
GP[27]	RESET_BT	out	Reset signal for Bluetooth	EXT_CLK	in
GP[26]	GPIO26	bi	not used	RXD	in
GP[25]	PWR_FAIL	in	Powerfail IRQ	TXD	out
GP[24]	$\overline{\text{PCD}}$	in	PCMCIA card detect	SFRM	out
GP[23]	GPIO23	in	TTL I/O IRQ	SCLK	out

TABLE 3.

GPIOs of PXA255 (Trizeps III) used on ConXS and their alternate functions

PXA255 Pin	Function on ConXS	Dir	Description	Alternate function	Dir
GP[22]	internally used on Trizeps III	-			
GP[21]	TTLIO_IRQ	in	IRQ TTLIO		
GP[20]	$\overline{\text{IRQ\_HIL}}$	in	IRQ Hilscher	DREQ[0]	in
GP[19]	internally used on Trizeps III	-		DREQ[1]	in
GP[18]	RDY	in	External bus ready	RDY	in
GP[17]	GPIO17	bi	Extension bus header	PWM1	out
GP[16]	GPIO16	bi	Extension bus header	PWM0	out
GP[15]	$\overline{\text{CS1}}$	out	Active low chip select 1	nCS[1]	out
GP[14]	GPIO14	bi	Extension bus header	MBREQ	in
GP[13]	GPIO13	bi	Extension bus header	MBGNT	out
GP[12]	MMC_DET	in	MMC detection	32 kHz	out
GP[11]	GPIO11	bi	Extension bus header	3.6 MHz	out
GP[10]	IRQ_USB_SL	in	Interrupt USB-Slave	RTCCLK	out
GP[9]	GPIO09	bi	Extension bus header	MMCCS1	out
GP[8]	MMC_CS0	out	MMC Chip select 0	MMCCS0	out
GP[7]	GPIO07	bi	Extension bus header	48 MHz clock	out
GP[6]	MMC_CLK	out	MMC clock	MMCCLK	out
GP[5]	internally used on Trizeps III	-			
GP[4]	internally used on Trizeps III	-			
GP[3]	internally used on Trizeps III	-			
GP[2]	internally used on Trizeps III	-			
GP[1]	PRDY	in	PCMCIA IRQ	GP_RST	in
GP[0]	IRQ_PIC	in	PIC IRQ		

### 3.10 Ethernet

The Ethernet Controller on Trizeps III board (DM9000 by Davicom) provides 10 / 100MBit interface

### 3.11 UART serial ports

The ConXS provides four kinds of serial ports:

- USB
- Bluetooth
- Standard
- Full Function

- Network SSP

### 3.11.1 USB Device Controller - UART

The universal serial bus device controller (UDC) supports three endpoints and can operate half-duplex at a baud rate of 12 Mbps (slave only, not a host or hub controller). The UDC is USB-compliant and supports all standard device requests issued by the host. The external pins dedicated to this interface are UDC+ and UDC-. The USB protocol uses differential signalling between the two pins for half-duplex data transmission. A 1.5 KOhm resistor is connected between GPIO22 and the USB cable's D+ signal to pull the UDC+ pin high when not driven. This signifies the UDC is a high-speed, 12 Mbps device and provides the correct polarity for data transmission.

The UDC is accessible by an USB-B connector. However, the user should refer to the Universal Serial Bus Specification, Revision 1.0<sup>1</sup> for a full description of the USB protocol and its operation.

### 3.11.2 Bluetooth - UART

The Bluetooth UART is either used with a Bluetooth module (WML-C20AB or WML-C10 on the bottom side of the ConXS) or it is configured as an universal asynchronous receiver / transmitter (UART) serial controller. A Maxim MAX3223 RS232 transceiver is used to manage the level conversion and line interface. The device has a power saving automatic shutdown that powers down the chip if no valid RS232 levels are detected. The component may also be forced off by the FORCEON signal. The Bluetooth UART is accessible by connector J18 (10-pin header). The external pins dedicated to this interface are TXD1, RXD1, RTS1 and CTS1.

For the communication between the PC (DB9 male) and the ConXS a serial extension cable is needed. Therefore the serial port J18 (10 pin header) is to be connected with a short flat cable to a DB9 female connector (see figure 7 on page 36).

### 3.11.3 Standard UART

The STUART can be used as an IrDA interface. The infrared communications port (ICP) operates at half-duplex and provides direct connection to commercially available Infrared Data Association (IrDA) compliant LED transceivers. The ICP supports both the original IrDA standard with speeds up to 115.2 Kbps as well as the newer 4-Mbps standard. Both standards use different bit encoding techniques and serial packet formats. Low-speed IrDA transmission uses the Hewlett-Packard Serial Infrared standard (HP-SIR) for bit encoding and an UART as the serial engine; high-speed uses Four-Position Pulse Modulation (4PPM) and a specialized serial packet protocol developed expressly for IrDA transmission. Standard UART is accessible by connector J20 (10-pin header). The external pins dedicated to the ICP are TXD2 and RXD2, IRDA\_MODE and IRDA\_SD are connected to the CPLD.

---

1. The latest revision of the Universal Serial Bus Specification Revision 1.0 can be accessed via the World Wide Web Internet side at: <http://www.teleport.com/~usb/>

FIGURE 4. Sample: Use of IrDA

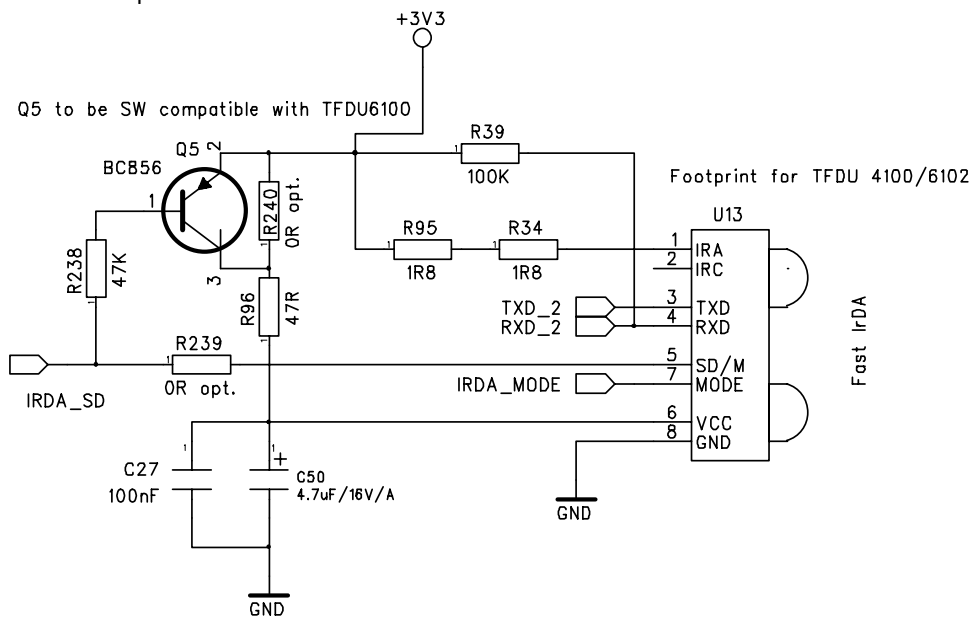


TABLE 4. IrDA Control Register

Offset 0x02400000														IrDA Control Register		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	1
Reserved															IRDA_MODE	IRDA_SD
Bits	Name		Type	Description												
0	IRDA_SD		Write Only	IrDA Shutdown 0 - IrDA activ 1 - IrDA inactiv												
1	IRDA_MODE		Write Only	IrDA Mode 0 - Low speed 1 - High speed												

Alternately you can use serial port 2 as an UART.

#### 3.11.4 Full Function UART

A Maxim MAX3243 RS232 transceiver is used to manage the level conversion and line interface. The device has a power saving automatic shutdown that powers down the chip if no valid RS232 levels are detected. The component may also be forced off by the FORCEON signal. Full Function UART is accessible by the male serial port connector J5 (DSUB9M). This port provides RTS, CTS, DSR, DTR, DCD and RI modem signals to support a serial IO port PC synchronous application.

#### 3.11.5 Network SSP Serial Port

The NSSP is a synchronous serial interface that connects to a variety of external analog-to-digital (A/D) converters, telecommunication CODECs, and many other devices that use serial protocols for data transfer. The NSSP provides support for the following protocols:

- Texas Instruments (TI) Synchronous Serial Protocol
- Motorola Serial Peripheral Interface (SPI) protocol
- National Semiconductor Microwire
- Programmable Serial Protocol (PSP)

The NSSP operates as full-duplex devices for the TI Synchronous Serial Protocol, SPI, and PSP protocols and as a half-duplex devices for the Microwire devices.

The external pins dedicated to this interface are NSSPTXD, NSSPRXD, NSSPCLK and NSSPFRM. The NSSP is accessible by the extension connector J2.

#### 3.12 TTL I/O

ConXS offers 8 TTL Inputs and 8 TTL Outputs. The TTL Outputs are accessible by the connector J1, the TTL Inputs by the connector J2. The output signals (OUTPUT[0:7]) correspond with dataline signals D[0:7], which are switched by a CPLD. They will be selected by addressing 0x19800000 (\CS\_IO\_OUT and \CS\_IO\_IN). The Inputs can be read as follows:

```
read = *(short *) ADR
```

The Outputs can be written as follows:

```
*(short *) portadr = value
```

#### 3.13 Audio In/Out

The Trizeps III board includes a single chip integrated mixed signal audio and telecom codec (Philips UCB 1400). JJ2 and JJ3 on the ConXS give access to the speaker and microphone signals. The pinout of JJ2 is shown in table 24 on page 38 and of JJ3 in table 25 on page 38.

The ConXS is additionally fitted out with 3.5mm jack chassis sockets for stereo headphone and microphone.

#### 3.14 Display connector, 4 wire Touch Panel, contrast EEPOT and backlight switch

The PXA255 on Trizeps III offers a 16 bit LCD-controller. The audio and telecom codec (see chapter 3.13, "Audio In/Out" on page 14) provides also a 4 wire touch screen interface. The relevant signals are accessible at J14 see table 18 on page 34.

The backlight voltage can be switched by the L\_DISP signal (CPLD, see BCR). The backlight voltage can either be switched to input voltage or to +5V. This depends of the inverter type.

The contrast voltage can be adjusted by an Digitally-Controlled Potentiometer by Xicor. The device consists of a resistor array, wiper switches, a control section, and nonvolatile memory. The wiper position is controlled by a three-wire interface.

The potentiometer is implemented by a resistor array composed of 99 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the CS, U/D, and INC inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

TABLE 5.

Display Contrast Register

Offset 0x03800000														Display Contrast Register		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	1	1
Reserved														EEPOT_U_D	EEPOT_INC	EEPOT_CS
Bits	Name		Type	Description												
0	EEPOT_CS		Write Only	Chip Select of EEPOT 0 - activ 1 - inactiv												
1	EEPOT_INC		Write Only	Increment of EEPOT 0 - increment by 1 1 - inactive												
2	EEPOT_U_D		Write Only	Direction (Up/Down)of EEPOT 0 - decrement 1 - increment												

All of these signals are available at the 40-pin connector J14 (description: table 18 on page 34).

**3.15 SD / MMC connector**

The MultiMediaCard standard grew out of a joint development between SanDisk Corporation and Siemens AG/Infineon Technologies AG, and was introduced in November 1997. MultiMediaCards weigh less than two grams and, about the size of a postage stamp, are the world’s smallest (24mm x 32mm x 1.4 mm) removable solid-state memory solutions for mobile applications. These convenient, reliable, rugged and lightweight standardized data carriers store up to 64 MBytes.

MultiMediaCards use ROM technology for read-only applications and Flash technology for read/write applications. The cards are fast for excellent system perfor-



TABLE 6.

UPS Register

Offset 0x02800000															UPS Register				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Reset	?	?	?	?	?	?	?	?	?	?	?	0	1	1	0	0			
Reserved												BATT_EMPTY	AUTO_DSPL_OFF	AUTO_PWR_OFF	CHARGE	BATT_EN			
Bits	Name		Type	Description															
0	BATT_EN		Output R/W	External battery enable signal 0 - external battery OFF 1 - external battery ON															
1	CHARGE		Output R/W	Charge external battery 0 - Do not charge 1 - Charge															
2	AUTO_PWR_OFF		Flag R/W	Turn off system flag 0 - OS does not power down after powerfail-IRQ 1 - OS powers down after powerfail-IRQ															
3	AUTO_DSPL_OFF		Flag R/W	Turn off backlight inverter flag 0 - Leave backlight ON 1 - Powerfail-IRQ handler switches backlight OFF															
4	BATT_EMPTY		Input Read Only	External battery status 0 - External battery empty 1 - External battery full															

### 3.18 USB Host connector

The Trizeps III is featured by Transdimension's high performance embedded USB host/slave controller. This controller is capable of the USB 2.0 OTG protocol and has a maximal Bitrate of 12MB. The chip is optimized to generate minimal CPU overhead.

ConXS offers a double USB A connector (J12) to connect mouse, keyboard, memory cards or others. Alternately you can use one of this ports to get USB OTG by an 5-pin Header (J21)

**3.19 NV-SRAM**

ConXS can be fitted out with a Non-Volatile SRAM K6X4016T3F by Samsung. It is a Low Power and Low Voltage CMOS Static RAM organized as 256Kx16 bit. The SRAM is optional and usually not placed. The SRAM is supplied from an external battery.

**3.20 Hilscher COM-Module connector**

ConXS offers an 50-pin high density connector for Hilscher-COM modules. You can find the pin description on table 9 on page 28.

**3.21 Extension bus connector**

Con XS offers a second 50-pin high density connector as extension bus. You can find the pin description on table 10 on page 30.

## Appendix A

In this chapter you can find detailed description about all headers and connectors on ConXS.

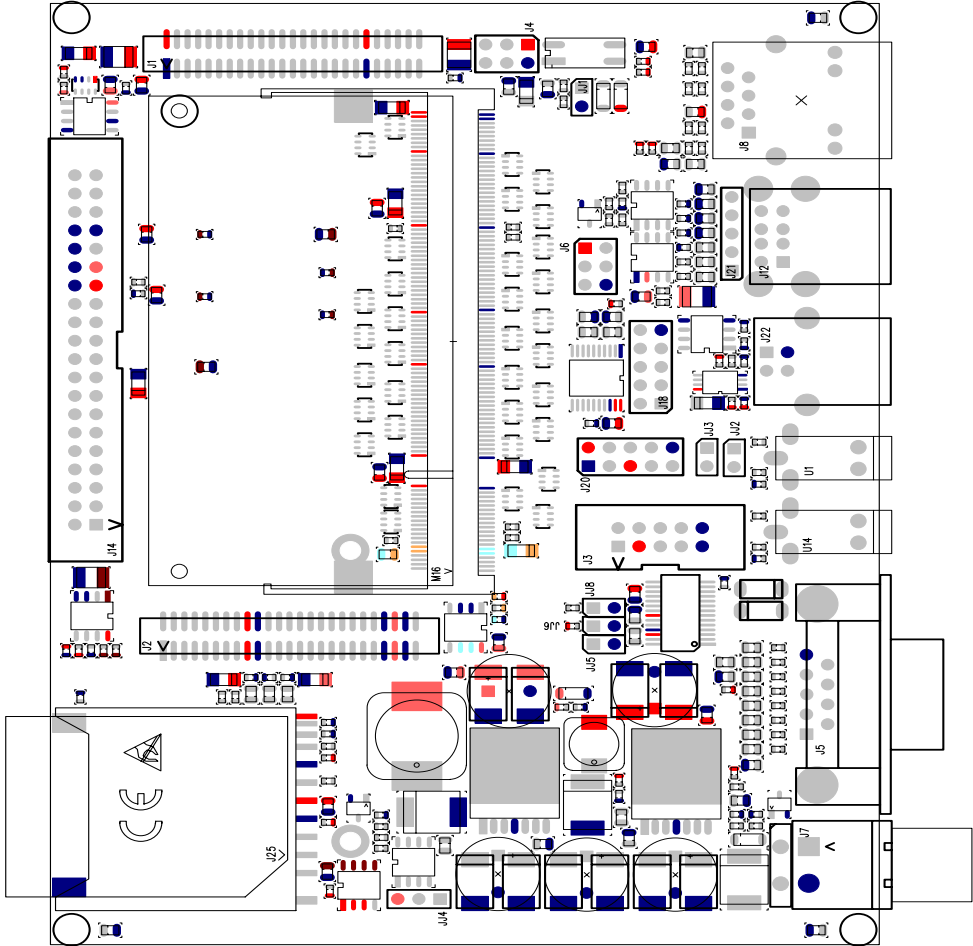
## A.1 Overview of all jumpers, connectors

TABLE 7.

Overview of all jumpers and connectors

Name	Function	Type
M16	Trizeps III connector	
J1	Hilscher COM-Module connector	Samtec FTSH-125-01-LDV
J2	Extension bus connector	Samtec FTSH-125-01-LDV
J3	Uninterruptible Power Supply (UPS) connector	Header SL2-10
J4	JTAG connector (CPLD)	Header SL2-6
J5	RS232 connector (port 3)	DSUB9 male
J6	Bluetooth programmable connector	Header SL2-6 (optional)
J7	Power Supply	Phoenix MSTBA2,5/2-G-5.08
J8	Ethernet RJ45 connector	HFJ11-2450E-L12
J12	USB-A connector	AMP 787617-x
J14	Display connector	Header SL2-40
J18	RS232 connector (port 1)	Header SL2-10
J20	IrDA connector / DIAG Hilscher	Header SL2-10
J21	USB Mini-AB (OTG)	Header SL1-5
J22	USB-B connector	Reichelt USB PCB BW
J25	SD / MMC card connector	Yamaichi Electronics FPS009-2405
JJ1	Battery connector	Header SL1-2
JJ2	Speaker connector	Header SL1-2
JJ3	Microphone connector	Header SL1-2
JJ4	Backlight power select connector	Header SL1-3
JJ5	Reset connector	Header SL1-2
JJ6	Code select CPLD connector	Header SL1-2
JJ8	Angelboot connector	Header SL1-2
U1	Headphone connector	JISC 150301
U7	Compact Flash connector	3M N7E50-7516-xx
U14	Microphone connector	JISC 150301

FIGURE 6. Jumper and connector locations (top side)



## A.2 Trizeps III Connector M16

In the following you find the pinout of the Trizeps III socket.

**TABLE 8.**

M16 - Trizeps III connector

Pin	Name	Description
1	MIC_OUT	microphone input signal
2	AD3	analog voltage input (UCB 1400)
3	MIC_GND	microphone ground switch input
4	VIN_AD2	analog voltage input (UCB 1400) <sup>a</sup>
5	LINEIN_L	Line in left channel (UCB1400)
6	AD1	analog voltage input (UCB 1400)
7	LINEIN_R	Line in right channel (UCB1400)
8	VBAT_AD0	analog voltage input (UCB 1400)
9	VSSA_AUDIO	Analog ground audio (UCB 1400)
10	VDDA_AUDIO	Analog power audio (UCB 1400)
11	VSSA_AUDIO	Analog ground audio (UCB 1400)
12	VDDA_AUDIO	Analog power audio (UCB 1400)
13	HEADPHONE_GND	Line out ground output (UCB 1400)
14	TSPX	positive X-plate touch screen (UCB 1200)
15	HEADPHONE_L	Line out left channel (UCB1400)
16	TSMX	negative X-plate touch screen (UCB 1200)
17	HEAPHONE_R	Line out right channel (UCB 1400)
18	TSPY	positive Y-plate touch screen (UCB 1200)
19	RXD_2	serial port two receive pin (IrDA) (PXA 255)
20	TSMY	negative Y-plate touch screen (UCB 1200)
21	TXD_2	serial port two transmit pin (IrDA) (PXA 255)
22	VDD_FAULT	not used
23	FF_DTR	Full Function UART Data Terminal Ready
24	BATT_FAULT	not used
25	FF_CTS	Full Function UART Clear To Send
26	RESET_IN	reset input
27	FF_RTS	Full Function UART Ready To Send
28	TUDC-	serial port zero bidirectional (UDC) (PXA 255)
29	FF_DSR	Full Function UART Data Set Ready
30	TUDC+	serial port zero bidirectional (UDC) (PXA 255)
31	FF_DCD	Full Function UART Data Carrier Detect
32	BT_CTS	BlueTooth UART Clear To Send
33	FF_RXD	Full Function UART Receive Data
34	BT_RTS	BlueTooth UART Ready To Send
35	FF_TXD	Full Function UART Transmit Data
36	BT_RXD	BlueTooth UART Receive Data

TABLE 8.

M16 - Trizeps III connector

Pin	Name	Description
37	FF_RI	Full Function UART Ring Indicator
38	BT_TXD	BlueTooth UART Transmit Data
39	GND	Ground
40	+3V3	Power Supply
41	GND	Ground
42	+3V3	Power Supply
43	GPIO00_IRQ_PIC	General purpose I/O
44	L_BIAS	LCD controller display data (PXA 255)
45	GPIO01_PRDY	General purpose I/O
46	LDD07	LCD controller display data (PXA 255)
47	GPIO06_MMC_CLK	General purpose I/O
48	LDD09	LCD controller display data (PXA 255)
49	GPIO07	General purpose I/O
50	LDD11	LCD controller display data (PXA 255)
51	GPIO08_MMC_CS0	General purpose I/O
52	LDD12	LCD controller display data (PXA 255)
53	GPIO09	General purpose I/O
54	LDD13	LCD controller display data (PXA 255)
55	GPIO10_IRQ_USB_SL	General purpose I/O
56	L_PCLK	LCD pixel clock (PXA 255)
57	GPIO11	General purpose I/O
58	LDD03	LCD controller display data (PXA 255)
59	GPIO12_MMC_DET	General purpose I/O
60	LDD02	LCD controller display data (PXA 255)
61	GPIO13	General purpose I/O
62	LDD08	LCD controller display data (PXA 255)
63	GPIO14	General purpose I/O
64	LDD15	LCD controller display data (PXA 255)
65	GPIO16	General purpose I/O
66	LDD14	LCD controller display data (PXA 255)
67	GPIO17	General purpose I/O
68	L_LCLK	LCD line clock (PXA 255)
69	GPIO20/IRQ_HIL	General purpose I/O
70	LDD01	LCD controller display data (PXA 255)
71	GPIO21_TTLIO_IRQ	General purpose I/O
72	LDD05	LCD controller display data (PXA 255)
73	GPIO32	General purpose I/O
74	LDD10	LCD controller display data (PXA 255)
75	GPIO23	General purpose I/O

TABLE 8.

M16 - Trizeps III connector

Pin	Name	Description
76	LDD00	LCD controller display data (PXA 255)
77	GPIO24_PCD	General purpose I/O
78	LDD04	LCD controller display data (PXA 255)
79	GPIO25_POWERFAIL	General purpose I/O
80	LDD06	LCD controller display data (PXA 255)
81	GPIO26	General purpose I/O
82	L_FCLK	LCD frame clock (PXA 255)
83	GND	Ground
84	+3V3	Power Supply
85	GPIO27_RESET_BT	General purpose I/O
86	NSSPFRM	Network Synchronous Serial port frame (PXA 255)
87	RESET_OUT	Reset output (PXA 255)
88	NSSPCLK	Network Synchronous Serial port clock
89	WE	Memory Write Enable (PXA 255)
90	NSSPRXD	Network Synchronous Serial port receive
91	OE	Memory Output Enable (PXA 255)
92	NSSPTXD	Network Synchronous Serial port transmit
93	RD/WR	read/write direction control for memory bus (PXA255)
94	PCE1	PCMCIA card enable (low-byte lane) (PXA 255)
95	GPIO18/RDY	not used
96	PCE2	PCMCIA card enable (high-byte lane) (PXA 255)
97	POE	PCMCIA output enable (PXA 255)
98	PREG	PCMCIA register select (PXA 255)
99	PWE	PCMCIA write enable (PXA 255)
100	PSKTSEL	PCMCIA socket select (PXA 255)
101	PIOW	PCMCIA I/O write (PXA 255)
102	PWAIT	PCMCIA wait (PXA 255)
103	PIOR	PCMCIA I/O read (PXA 255)
104	PIOIS16	I/O select 16 (PXA 255)
105	CS1	static chip select (PXA 255)
106	CS4	static chip select (PXA 255)
107	CS3	static chip select (PXA 255)
108	+3V3	Power Supply
109	GND	Ground
110	A08	memory address bus (PXA 255)
111	A00	memory address bus (PXA 255)
112	A09	memory address bus (PXA 255)
113	A01	memory address bus (PXA 255)

TABLE 8.

M16 - Trizeps III connector

Pin	Name	Description
114	A10	memory address bus (PXA 255)
115	A02	memory address bus (PXA 255)
116	A11	memory address bus (PXA 255)
117	A03	memory address bus (PXA 255)
118	A12	memory address bus (PXA 255)
119	A04	memory address bus (PXA 255)
120	A13	memory address bus (PXA 255)
121	A05	memory address bus (PXA 255)
122	A14	memory address bus (PXA 255)
123	A06	memory address bus (PXA 255)
124	A15	memory address bus (PXA 255)
125	A07	memory address bus (PXA 255)
126	DQM0	not used
127	$\overline{\text{OTG\_EXTVB0}}$	Turn on/off the external Vbus for OTG operation
128	DQM1	not used
129	$\overline{\text{OTG\_PO}}$	Turn on/off the gang power for all host ports
130	DQM2	not used
131	$\overline{\text{OTG\_OC}}$	Over current condition indicator for gang powered host ports
132	DQM3	not used
133	OTG_VBP	Vbus pulsing control
134	A25	memory address bus (PXA 255)
135	OTG_VBUS	Vbus input sampled during HNP/SRPOperations by the OTG port
136	A24	memory address bus (PXA 255)
137	OTG_ID	Connected to the ID-pin of the Mini-AB connector for OTG applications
138	A23	memory address bus (PXA 255)
139	OTG_DP2	Data line for Port 2
140	A22	memory address bus (PXA 255)
141	OTG_DM2	Data line for Port 2
142	A21	memory address bus (PXA 255)
143	OTG_DP1	Data line for Port 1
144	A20	not used
145	OTG_DM1	Data line for Port 1
146	A19	not used
147	GND	Ground
148	+3V3	Power Supply
149	D00	memory data (PXA 255)
150	D16	not used

TABLE 8.

M16 - Trizeps III connector

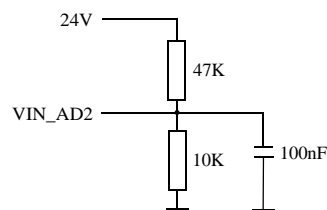
Pin	Name	Description
151	D01	memory data (PXA 255)
152	D17	not used
153	D02	memory data (PXA 255)
154	D18	not used
155	D03	memory data (PXA 255)
156	D19	not used
157	D04	memory data (PXA 255)
158	D20	not used
159	D05	memory data (PXA 255)
160	D21	not used
161	D06	memory data (PXA 255)
162	D22	not used
163	D07	memory data (PXA 255)
164	D23	not used
165	D08	memory data (PXA 255)
166	D24	not used
167	D09	memory data (PXA 255)
168	D25	not used
169	D10	memory data (PXA 255)
170	D26	not used
171	D11	memory data (PXA 255)
172	D27	not used
173	D12	memory data (PXA 255)
174	D28	not used
175	D13	memory data (PXA 255)
176	D29	not used
177	D14	memory data (PXA 255)
178	D30	not used
179	D15	memory data (PXA 255)
180	D31	not used
181	GND	Ground
182	+3V3	Power Supply
183	$\overline{\text{ETH\_LINK\_AKT}}$	Link LED signal
184	A18	memory address bus (PXA 255)
185	$\overline{\text{ETH\_SPEED100}}$	Speed LED signal
186	A17	memory adress bus (PXA 255)
187	ETH_TX0-	TP TX Output
188	A16	memory adress bus (PXA 255)
189	ETH_TX0+	TP TX Output

TABLE 8.

M16 - Trizeps III connector

Pin	Name	Description
190	MMC_CMD	MultiMedia card command
191	ETH_AGND	Analog Ground
192	MMC_DAT	MultiMedia Card data
193	ETH_RXI-	TP RX Input
194	I2C_DATA	I <sup>2</sup> C bus data
195	ETH_RXI+	TP RX Input
196	I2C_CLK/ANGBOOT	I <sup>2</sup> C bus clock
197	GND	Ground
198	+3V3	Power Supply
199	GND	Ground
200	+3V3	Power Supply

a. For an input voltage of 24V VIN\_AD2 is about 4.21V



### A.3 Hilscher COM-Module connector

TABLE 9.

J1 - Hilscher COM-Module connector

Pin	Signal	Description	Direction
1	GND	Ground	-
2	+3V3	Power Supply	-
3	OUTPUT1/BD01	TTL Output 01 / buffered data line 01	out / bi
4	OUTPUT0/BD00	TTL Output 00 / buffered data line 00	out / bi
5	OUTPUT3/BD03	TTL Output 03 / buffered data line 03	out / bi
6	OUTPUT2/BD02	TTL Output 02 / buffered data line 02	out / bi
7	OUTPUT5/BD05	TTL Output 05 / buffered data line 05	out / bi
8	OUTPUT4/BD04	TTL Output 04 / buffered data line 04	out / bi
9	OUTPUT7/BD07	TTL Output 07 / buffered data line 07	out / bi
10	OUTPUT6/BD06	TTL Output 06 / buffered data line 06	out / bi
11	BA02/A2D1	buffered address line 02 / multiplexed line	out / bi
12	BA01/A1D0	buffered address line 01 / multiplexed line	out / bi
13	BA04/A4D3	buffered address line 04 / multiplexed line	out / bi
14	BA03/A3D2	buffered address line 03 / multiplexed line	out / bi
15	BA06/A6D5	buffered address line 06 / multiplexed line	out / bi
16	BA05/A5D4	buffered address line 05 / multiplexed line	out / bi
17	BA08/A8D7	buffered address line 08 / multiplexed line	out / bi
18	BA07/A7D6	buffered address line 07 / multiplexed line	out / bi
19	BA10	buffered address line 10	out
20	BA09	buffered address line 09	out
21	BA12	buffered address line 12	out
22	BA11	buffered address line 11	out
23	BA14	buffered address line 14	out
24	BA13	buffered address line 13	out
25	$\overline{\text{BWE}}$	buffered write enable	out
26	$\overline{\text{CS\_HIL}}$	chip select Hilscher	out
27	$\overline{\text{GPIO20/IRQ\_HIL}}$	interrupt request Hilscher	in
28	$\overline{\text{BOE}}$	buffered output enable	out
29	$\overline{\text{RST\_OUT\_BUF}}$	buffered RESET_OUT	out
30	$\overline{\text{BUSY}}$	busy signal Hilscher	out
31	DIAG_RX0	diagnostic receive Hilscher	in
32	DIAG_TX0	diagnostic transmit Hilscher	out
33	-	reserved	-
34	-	reserved	-
35	-	reserved	-
36	-	reserved	-
37	-	reserved	-
38	-	reserved	-

**TABLE 9.**

J1 - Hilscher COM-Module connector

Pin	Signal	Description	Direction
39	GND	Ground	-
40	+3V3	Power Supply	-
41	-	reserved	-
42	-	reserved	-
43	-	reserved	-
44	-	reserved	-
45	-	reserved	-
46	-	reserved	-
47	-	reserved	-
48	-	reserved	-
49	-	reserved	-
50	(GND)	usually not connected	-

#### A.4 Extension bus connector

TABLE 10.

J2 - Extension bus connector

Pin	Signal	Description	Direction
1	BD08	buffered data line 08	bi
2	INPUT07	TTL Input 07	in
3	BD09	buffered data line 09	bi
4	INPUT06	TTL Input 06	in
5	BD10	buffered data line 10	bi
6	INPUT05	TTL Input 05	in
7	BD11	buffered data line 11	bi
8	INPUT04	TTL Input 04	in
9	BD12	buffered data line 12	bi
10	INPUT03	TTL Input 03	in
11	BD13	buffered data line 13	bi
12	INPUT02	TTL Input 02	in
13	BD14	buffered data line 14	bi
14	INPUT01	TTL Input 01	in
15	BD15	buffered data line 15	bi
16	INPUT00	TTL Input 00	in
17	+3V3	Power Supply	-
18	+3V3	Power Supply	-
19	GND	Ground	-
20	GND	Ground	-
21	AD1	Analog / Digital Input 1 (UCB1400)	in
22	EXT_CLK	External Clock for CPLD	in
23	AD3	Analog / Digital Input 3 (UCB1400)	in
24	GP07	General purpose IO 07 (PXA255)	bi
25	GP23	General purpose IO 23 (PXA255)	bi
26	GP09	General purpose IO 09 (PXA255)	bi
27	GP21_TTLIO_IRQ	General purpose IO 21 (PXA255)	bi
28	GP11	General purpose IO 11 (PXA255)	bi
29	NSSPTXD	Network Synchronous Serial port transmit	out
30	GP13	General purpose IO 13 (PXA255)	bi
31	NSSPRXD	Network Synchronous Serial port receive	in
32	GP14	General purpose IO 14 (PXA255)	bi
33	NSSPCLK	Network Synchronous Serial port clock	in
34	GP16	General purpose IO 16 (PXA255)	bi
35	NSSPFRM	Network Synchronous Serial port frame	in
36	GP17	General purpose IO 17 (PXA255)	bi
37	$\overline{CS4}$	chip select 4	out

TABLE 10.

J2 - Extension bus connector

Pin	Signal	Description	Direction
38	GP22	General purpose IO 22 (PXA255)	bi
39	-	reserved for future use	-
40	-	reserved for future use	-
41	-	reserved for future use	-
42	-	reserved for future use	-
43	GND	Ground	-
44	GND	Ground	-
45	+5V	Power Supply	-
46	+5V	Power Supply	-
47	GND	Ground	-
48	GND	Ground	-
49	VIN_FUSED	Power Supply	-
50	VIN_FUSED	Power Supply	-

#### A.5 UPS connector

An UPS is available for the ConXS. The UPS is connected with ConXS via the following connector.

TABLE 11.

J3 - UPS connector

Pin	Signal	Description
1	I2C_DATA	data I <sup>2</sup> C Bus (SDA of PXA255)
2	I2C_CLK / ANGBOOT	clock I <sup>2</sup> C Bus (SCL of PXA255)
3	+3V3	Power Supply
4	BATT_EMPTY	CPLD signal
5	BATT_EN	CPLD signal
6	CHARGE	CPLD signal
7	VIN_FUSED	Power Supply
8	VIN_FUSED	Power Supply
9	GND	Ground
10	GND	Ground

### A.6 JTAG connector (CPLD)

A CPLD is placed on the ConxS which can be programmed through an 6-pin header with the following pinout.

TABLE 12.

J4 - JTAG connector (CPLD)

Pin	Signal	Description
1	+3V3	Power Supply
2	GND	Ground
3	XC_TCK	Clock signal
4	XC_TDO	Output signal
5	XC_TDI	Input signal
6	XC_TMS	Mode signal

### A.7 RS232 connector (port 3)

The connector J5 is a male DB9 connector with the following pin description.

TABLE 13.

J5 - Serial Interface connector (port 3)

Pin	Signal	Description
1	FF_DCD_V24X	Data Carrier Detect
2	FF_RXD_V24X	Receive Data
3	FF_TXD_V24X	Transmit Data
4	FF_DTR_V24X	Data Terminal Ready
5	GND	Ground
6	FF_DSR_V24X	Data Set Ready
7	FF_RTS_V24X	Request to Send
8	FF_CTS_V24X	Clear to Send
9	FF_RI_V24X	Ring Indicator

### A.8 Bluetooth programmable connector

It is possible to program the Bluetooth module via SPI-interface with this connector

TABLE 14.

J6 - Bluetooth programmable connector

Pin	Signal	Description
1	+3V3	Power Supply
2	BT_SPI_CSB	Chip select for synchronous serial interface
3	BT_SPI_MISO	Synchronous serial interface data output
4	BT_SPI_MOSI	Synchronous serial interface data input

TABLE 14.

J6 - Bluetooth programmable connector

Pin	Signal	Description
5	BT_SPI_CLK	Synchronous serial interface clock
6	GND	Ground

### A.9 Power Supply (I)

The Power Supply connector is produced by PHOENIX. It's a 2 pin connector with the part number MSTBVA 2,5/2-G-5,08.

TABLE 15.

J7 - Power Supply

Pin	Signal	Description
1	VIN	Power Supply
2	GND	Ground

### A.10 Ethernet connector

The Ethernet connector is an usually RJ45 connector with integrated traffic LEDs with the following pin description.

TABLE 16.

J8 - Ethernet connector

Pin	Signal	Description
1	TD+	Transmit differential output
2	TD-	Transmit differential output
3	RD+	Receive differential output
4	CT_T	Center point transmit
5	CT_R	Center point receive
6	RD-	Receive differential output
7	nc	not connected
8	CHGND	Chassis ground
9	+3V3	pullup 1K
10	$\overline{\text{ETH\_SPEED\_100}}$	Status: Ethernet speed
11	+3V3	pullup 1K
12	$\overline{\text{ETH\_LINK\_AKT}}$	Status: Ethernet link

## A.11 USB-A connector

TABLE 17.

J12 - USB-A connector

Pin	Signal	Description
1	VCCB+	Power Supply
2	OTG_DM2	Differential signal
3	OTG_DP2	Differential signal
4	GNDB	Ground
5	VCCT+	Power Supply
6	OTG_DM1	Differential signal
7	OTG_DP1	Differential signal
8	GNDT	Ground
9	CHGND	Chassis Ground
10	CHGND	Chassis Ground
11	CHGND	Chassis Ground
12	CHGND	Chassis Ground

## A.12 Display connector

This is an universal LCD connector to connect displays from sub 1/4 VGA to 16bpp TFT SVGA, LVDS or DVI extensions available. table 18 on page 34 describes the pins and their functions.

TABLE 18.

J14 - Display connector (40-pin Header)

Pin	Signal	Description
1	LDD00	LCD controller display data (PXA255)
2	LDD01	LCD controller display data (PXA255)
3	LDD02	LCD controller display data (PXA255)
4	LDD03	LCD controller display data (PXA255)
5	LDD04	LCD controller display data (PXA255)
6	LDD05	LCD controller display data (PXA255)
7	LDD06	LCD controller display data (PXA255)
8	LDD07	LCD controller display data (PXA255)
9	LDD08	LCD controller display data (PXA255)
10	LDD09	LCD controller display data (PXA255)
11	LDD10	LCD controller display data (PXA255)
12	LDD11	LCD controller display data (PXA255)
13	LDD12	LCD controller display data (PXA255)
14	LDD13	LCD controller display data (PXA255)

TABLE 18.

J14 - Display connector (40-pin Header)

Pin	Signal	Description
15	LDD14	LCD controller display data (PXA255)
16	LDD15	LCD controller display data (PXA255)
17	L_FCLK	LCD frame clock (PXA255)
18	L_LCLK	LCD line clock (PXA255)
19	L_PCLK	LCD pixel clock (PXA255)
20	L_BIAS	LCD ac bias drive (PXA255)
21	TSMX	negative X-plate touch screen (Trizeps - UCB 1400)
22	TSMY	negative Y-plate touch screen (Trizeps - UCB 1400)
23	TSPX	positive X-plate touch screen (Trizeps - UCB 1400)
24	TSPY	positive Y-plate touch screen (Trizeps - UCB 1400)
25	L_DISP	LCD on
26	NC	not connected
27	+3V3	Power supply
28	GND	Ground
29	+5V	Power supply
30	GND	Ground
31	VIN_FUSED	Power supply
32	GND	Ground
33	GND	Ground
34	GND	Ground
35	I2C_DATA	Data I <sup>2</sup> C Bus (PXA255)
36	I2C_CLK	Clock I <sup>2</sup> C Bus (PXA255)
37	GPIO00_IRQ_PIC	Interrupt of the PIC (optional)
38	V_CONTRAST	Contrast voltage
39	NC	not connected
40	BL_POWER	Backlight power

### A.13 Serial port 1 connector

Signals of serial port 1 are available at this 10-pin header.

TABLE 19.

J18 - Serial port 1 connector

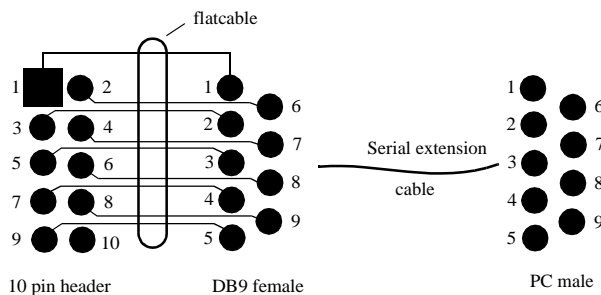
Pin	Signal	Description
1	-	internally connected to Pin 2 and 7
2	-	internally connected to Pin 1 and 7
3	COM2_TXD_V24	Transmit Data
4	COM2_CTS_V24	Clear To Send
5	COM2_RXD_V24	Receive Data

**TABLE 19.** J18 - Serial port 1 connector

Pin	Signal	Description
6	COM2_RTS_V24	Request To Send
7	-	internally connected to Pin 1 and 2
8	(+3V3)	(Power Supply)
9	GND	Ground
10	nc	not connected

If you want to connect J18 with a PC you can use the solution shown in figure 7 on page 36:

**FIGURE 7.** Connection of the serial interface header (J18) to the PC



**A.14 USB / IrDA connector**

USB and IrDA signals are available at connector J20.

**TABLE 20.** J20 - USB and IrDA Connector

Pin	Signal	Description
1	GND	Ground
2	+3V3	Power Supply
3	DIAG_RX0	diagnostic receive Hilscher
4	DIAG_TX0	diagnostic transmit Hilscher
5	+3V3	Power Supply
6	TXD_2	Transmit data
7	RXD_2	Receive data
8	IRDA_MODE	
9	IRDA_SD	
10	GND	Ground

---

**A.15 OTG connector**


---

TABLE 21.

J21 - OTG connector

Pin	Signal	Description
1	VCC+	Power Supply
2	OTG_DM2	differential signal
3	OTG_DP2	differential signal
4	OTG_ID	
5	GND	Ground

---

**A.16 USB-B connector**


---

TABLE 22.

J22 - USB-B connector

Pin	Signal	Description
1	VCC+	Power Supply
2	TUDC-	differential signal
3	TUDC+	differential signal
4	GND	Ground

---

**A.17 MultiMediaCard connector**


---

The MultiMediaCard connector has the following pinout:

Pin	Signal	Description
1	GPIO08_MMC_CS0	MMC chip select
2	MMC_CMD	MMC command
3	GND	Ground
4	+3V3	Power Supply
5	GPIO06_MMC_CLK	MMC clock
6	GND	Ground
7	MMC_DAT	MMC data
8	nc	not connected
9	nc	not connected
10	GND	100K pulldown
11	+3V3	Power Supply
12	GPIO12_MMC_DET	MMC detect (100K pulldown)
13	nc	not connected
14	GND	Ground

---

**A.18 Battery connector**

---

You can use this connector to supply the RTC and the SRAM with power.

---

**TABLE 23.**

JJ1 - Battery connector

Pin	Signal	Description
1	+3V3	Power Supply
2	GND	Ground

---

**A.19 Speaker connector**

---

Connect a speaker to JJ2.

---

**TABLE 24.**

JJ2 - Speaker connector

Pin	Signal	Description
1	HEADPHONE_R	Speaker positive signal
2	HEADPHONE_GND	Speaker negative signal

---

**A.20 Microphone connector**

---

Connect a microphone to JJ3.

---

**TABLE 25.**

JJ3 - Microphone connector

Pin	Signal	Description
1	MIC_OUT	Microphone output signal
2	MIC_GND	Microphone ground

---

**A.21 Backlight power select connector**

---

By setting this jumper you can decide to supply your backlight inverter with +5V or VIN-FUSED.

---

**TABLE 26.**

JJ4 - Backlight power select connector

Pin	Signal	Description
1	VIN_FUSED	Input voltage
2	BL_POWER	Backlight power
3	+5V	+5V supply

### A.22 Reset connector

For normal operation this jumper is left open. For resetting the board connect  $\overline{\text{RESIN}}$  to GND.

TABLE 27.

JJ5 - Reset connector

Pin	Signal	Description
1	GND	Ground
2	$\overline{\text{RESIN}}$	Reset in

### A.23 Code select connector

This is an jumper to set the CPLD

TABLE 28.

JJ6 - Code select connector

Pin	Signal	Description
1	CPLD_INPUT	100K pulled up
2	GND	Ground

### A.24 Angelboot

You can start the firmware by closing JJ8 when powering up.

TABLE 29.

JJ8 - Angel boot connector

Pin	Signal	Description
1	ANGELBOOT	Angel boot
2	GND	Ground

### A.25 Audio stereo connector

The audio stereo connector has the following pinout:

TABLE 30.

U1 - Audio stereo connector

Pin	Signal	Description
1	HEADPHONE_GND	Headphone Ground
2	HEADPHONE_L	Headphone left
3	HEADPHONE_R	Headphone right

## A.26 CompactFlash connector

TABLE 31.

U7 - CompactFlash Connector

Pin	Signal	Description
1	GND	Ground
2	S0_D03	Databus
3	S0_D04	Databus
4	S0_D05	Databus
5	S0_D06	Databus
6	S0_D07	Databus
7	$\overline{S0\_CE1}$	Card Enable signal
8	S0_A10	Memory address bus
9	S0_OE	Output Enable signal
10	S0_A09	Memory address bus
11	S0_A08	Memory address bus
12	S0_A07	Memory address bus
13	S0_VDD	Power Supply
14	S0_A06	Memory address bus
15	S0_A05	Memory address bus
16	S0_A04	Memory address bus
17	S0_A03	Memory address bus
18	S0_A02	Memory address bus
19	S0_A01	Memory address bus
20	S0_A00	Memory address bus
21	S0_D00	Databus
22	S0_D01	Databus
23	S0_D02	Databus
24	$\overline{S0\_IOIS}$	Write Protect signal
25	$\overline{S0\_CD2}$	Card Detect signal
26	$\overline{S0\_CD1}$	Card Detect signal
27	S0_D11	Databus
28	S0_D12	Databus
29	S0_D13	Databus
30	S0_D14	Databus
31	S0_D15	Databus
32	$\overline{S0\_CE2}$	Card Enable signal
33	$\overline{S0\_VS1}$	Voltage Sense signal
34	$\overline{S0\_IOR}$	I/O Read signal
35	$\overline{S0\_IOW}$	I/O Write signal
36	$\overline{S0\_WE}$	Write Enable signal
37	$\overline{S0\_RDY}$	Ready / Busy signal

TABLE 31.

U7 - CompactFlash Connector

Pin	Signal	Description
38	S0_VDD	Power Supply
39	nc	not connected
40	$\overline{S0\_VS2}$	Voltage Sense signal
41	S0_RESET	Reset signal
42	$\overline{S0\_WAIT}$	Wait signal
43	nc	not connected
44	$\overline{S0\_REG}$	Attribute-Memory-Select or Register signal
45	S0_BVD2	Battery Voltage Detect signal
46	S0_BVD1	Battery Voltage Detect signal
47	S0_D08	Databus
48	S0_D09	Databus
49	S0_D10	Databus
50	GND	Ground

### A.27 Microphone connector

The microphone connector has the following pinout:

TABLE 32.

U14 - Microphone connector

Pin	Signal	Description
1	MIC_GND	Microphone Ground
2	nc	not connected
3	MIC_OUT	Microphone out

---

**A.28 On board peripherals (address code)**

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**TABLE 33.**

On board peripherals

Offset ( $\overline{CS3}$ )	Device	Address Trizeps III
0x00000000	READ: PCMCIA Status	0x0C000000
0x00800000	R/W: SMSC91C96	0x0C800000
0x01000000	R/W: CAN SJA1000	0x0D000000
0x01800000	WRITE: TTL OUTPUT READ: TTL INPUT	0x0D800000
0x02000000	WRITE: PCMCIA CTL READ: PCMCIA STATUS	0x0E000000
0x02400000	WRITE: IrDA	0x0E400000
0x02800000	R/W: UPS	0x0E800000
0x03000000	RESERVED	0x0F000000
0x03800000	WRITE: EEPOT (display contrast)	0x0F800000

# Revision

Board: ConXS

TABLE 34.

Revision	PCB number	Date	Changes
1.0	01_01_04	28.03.2004	-----
1.1	01_01_04	02.09.2004	The signal name of Pin 73 of SODIMM200 is changed to GPIO32

FIGURE 8. Dimensions of ConXS board (top side)

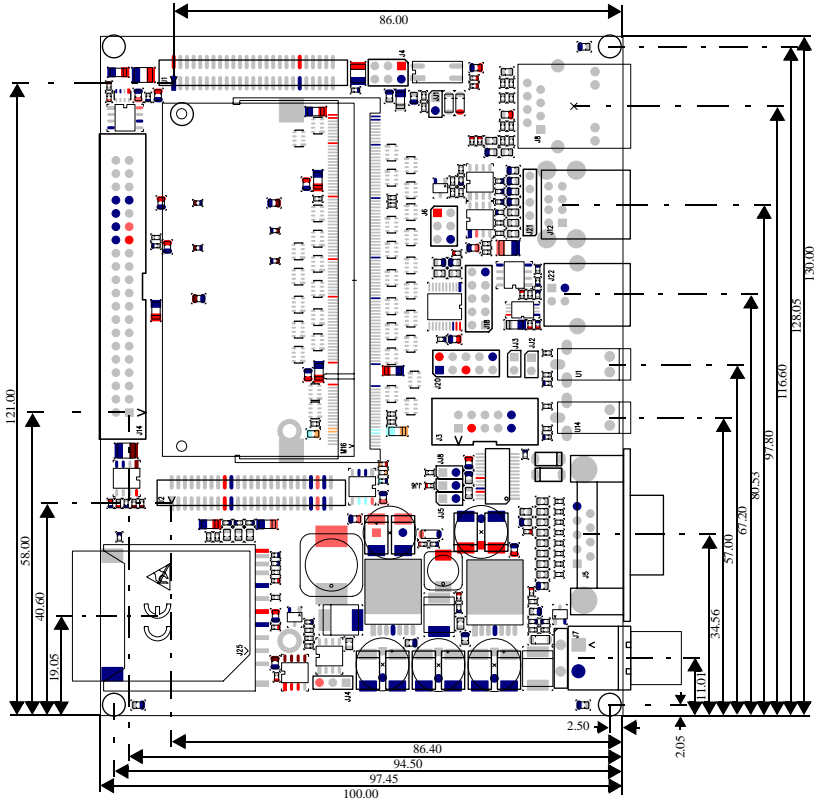


FIGURE 9. Dimension of ConXS board (bottom side)

