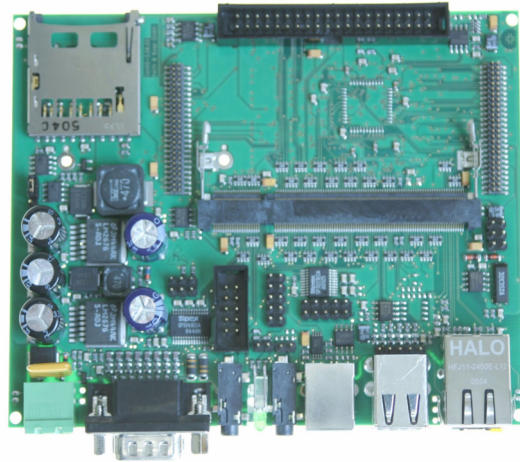


ConXS

Documentation 1.35



1.0 Introduction

The ConXS board is an industrial terminal based on Keith & Koep Trizeps IV¹ module, downwards compatible with the Trizeps III² module.

The board offers the following features:

- Ethernet: 10 / 100 MBit RJ45
- Compact Flash Socket Type II
- SD/MMC Card connector
- USB: e.g. 2 x USB host or 1 x USB host and 1 x OTG
- USB slave via PXA255 / PXA270
- Serial via DB9 male
- Serial via 10-pin Bluetooth, or Bluetooth module
- Serial via extension bus for IrDA or custom application
- Externally battery buffered Real Time Clock (RTC)
- Uninterruptible Power Supply interface (optional)
- NV-SRAM (optional)
- Headphone stereo out, Microphone-in mono
- single power supply (12V - 24V)
- Universal LCD connector from sub 1/4 VGA to 16bpp TFT SVGA, LVDS or DVI extensions available
- Contrast EEPROM

1. Keith & Koep GmbH offers Trizeps IV modules based on the Intel XScale PXA270 microprocessor. **(for more details download our Trizeps IV product brief <http://www.keith-koep.com/produkte/xscale-arm-embedded/trizeps4-product-brief.pdf>)**
2. Trizeps III module based on XScale PXA255 microprocessor. **(download our Trizeps III product brief <http://www.keith-koep.com/produkte/xscale-arm-embedded/trizeps3-product-brief.pdf>) <http://www.keith-koep.com>**

- Backlight switch
- Hilscher COM-Module connector
- Extension-bus routed through high density CPLD

2.0 Preface

2.1 Getting started

The ConXS board is designed as a motherboard for Trizeps III / IV based on XScale PXA255/270 prozessor. The first part of this chapter gives a physical description of the board and the second part describes:

1. How to unpack the board and how to make a visual inspection.
2. How to power up the board for the first time.
3. How to connect the board to a host system

2.1.1 Physical description

The physical layout of the board is shown in figure 6 on page 24 (You'll find details on the last page). The dimensions of the board are 130 x 100 mm (LxW). You can find all measures at figure 8 on page 48 and at figure 9 on page 49.

There is a number of header blocks on the board that accept 2-pin jumpers, allowing the board to be configured in different ways. Due to further header blocks it is possible to connect an LCD-display with touch screen. A serial connection to a host system is possible by using one of the RS232 interfaces.

2.1.2 Unpacking the board

The ConXS contains electronic components that are susceptible to electrostatic discharge (static electricity). To avoid electrostatic damage the board is supplied in an antistatic bag. When handling the card, risk of damage can be diminished by taking a few simple precautions:

1. Do not remove the card from the bag unless you are working on an antistatic, grounded surface and wearing an grounded antistatic wrist strap.
2. Keep the antistatic bag the card was supplied in; if you remove the card from a system, store it in the bag.

Normally ConXS is supplied with a Trizeps III or Trizeps IV in the SODIMM-socket. If the SODIMM is not fitted with a Trizeps module when you receive your board, follow the next instructions:

1. Slide the Trizeps into the socket taking account of the polarity mark. Do not touch the gold contacts. You can see that there is a polarization mark cut in the Trizeps ; this ensures that the module is adjusted correctly. Put the Trizeps module carefully at an angle of about 30 degrees into the socket.
2. Support the underside of the board and push the Trizeps down into the socket. It should click into its place with a gentle click.

Before you install and power up your ConXS, you should perform a short visual inspection:

1. Inspect the card for physical damage.

2. Ensure that each of the 2-pin jumpers is pushed down firmly onto its mounting posts. If you move any of the jumpers, refer to Appendix A to ensure they are replaced correctly.

2.1.3 Powering up the first time

Use Appendix A to ensure the jumpers are set appropriately. If you need more details on how to install the card or attach power supply, refer to Appendix A, too.

2.1.4 How to connect the board to host system

Use an RS232 null-modem cable to attach the serial interface on the board to an RS232 port on a terminal or terminal emulator. For example, you could connect it to a PC running Windows and use the Windows Terminal or Hyperterminal application. Configure the terminal to operate at 38 kbaud, 8-bit data, 1 stop bit, no parity, no flow control. If you need more details on choosing an appropriate cable, refer to appendix A.

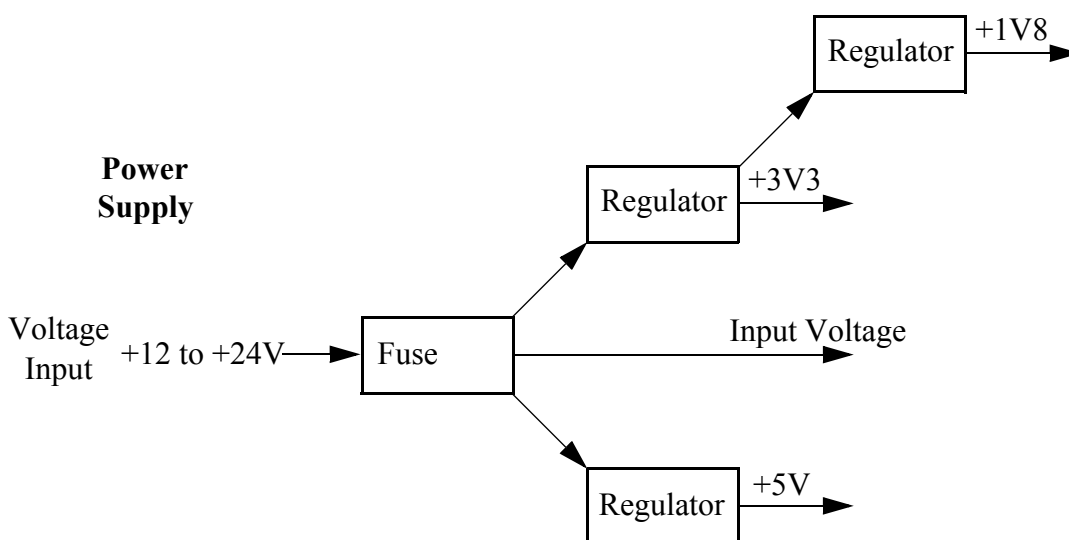
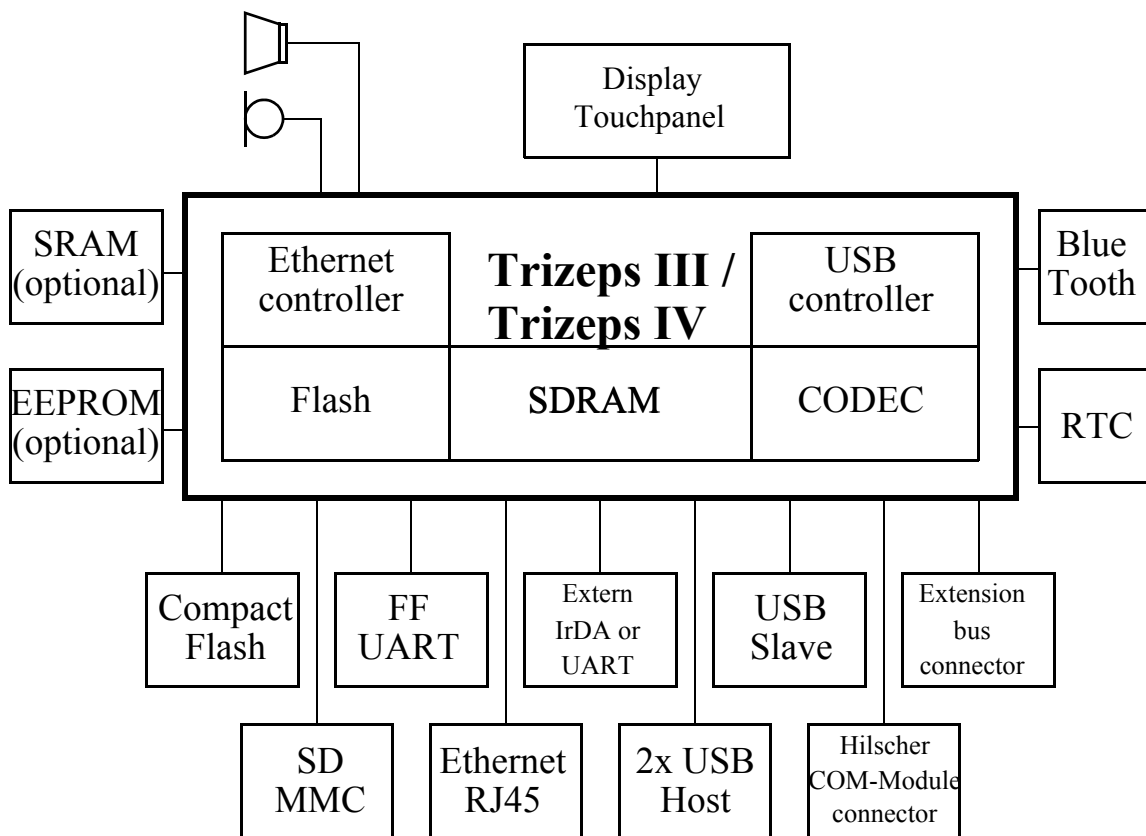
3.0 Functional specification

This chapter describes each functional element on the ConXS board. In the next chapters you can find more detailed information about the board and some important hints for programming it. The block diagram on figure 1 on page 4 shows the interconnections of the major elements.

Components of ConXS:

1. Trizeps III or Trizeps IV module
2. Serial EEPROM (optional)
3. Compact Flash socket type II
4. Board Control Register BCR
5. Real Time Clock
6. Reset
7. Power Supply
8. Power generation on board
9. GPIO
10. Ethernet
11. UART serial ports
12. TTL I/O
13. Audio in/out
14. Display connector, 4 wire Touch Panel, contrast EEPROM and backlight switch
15. SD / MMC connector
16. Powerfail - Interrupt
17. Uninterruptible Power Supply (UPS)
18. USB host
19. NV-SRAM
20. Contrast EEPROM
21. Backlight switch
22. Hilscher COM-Module connector
23. Extension bus

FIGURE 1. ConXS block diagram



3.1 Trizeps III module

The Trizeps III Module is based on the Intel® XScale™ PXA255 CPU (clock range from 100 to 400 MHz) which complies with the v.5TE ARM Architecture instruction set. The CPU is based on Intel® Superpipelined RISC technology utilizing advanced Intel 0.18μ process for high core speeds at low power (480K Dhrystone 2.1 per second @ 400 MHz).

Features of the Trizeps III module amongst others are :

- up to 64MB Flash memory (16 or 32 Bit)
- up to 128 MB SRAM (16 or 32 Bit)
- PCMCIA/Compact Flash Controller with 100 MHz memory bus
- LCD Controller
- Philips UCB1400 chip for audio, touch screen and power management
- Ethernet Controller 10/100 MBit
- USB Host Controller OTG242

3.2 Trizeps IV module

The Trizeps IV module is based on Intel® XScale™270 processor, which provides a clock range from 312 to 520 MHz and complies with the v.5TE ARM Architecture instruction set. PXA270 offers more features than the forerunner PXA255 : 256 Kbytes internal SRAM, camera interface, USB host, keypad interface. Additional features (except for Trizeps III features) of the Trizeps IV modules :

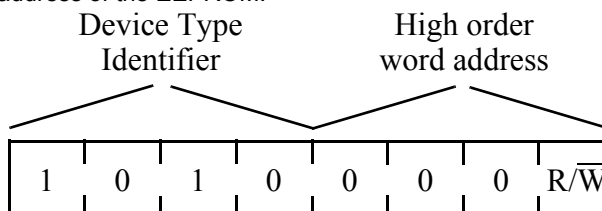
- optional 128MB NAND-Disk-On-Chip with integrated management logic
- up to 192 MB combined Flash (NOR + NAND)
- Camera interface

3.3 Serial EEPROM (optional)

ConXS provides a serial EEPROM (X24C16- Xicor) to be used as a non-volatile memory. It has a size of 16KBit and it is internal organized as 2048 x 8. The X24C16 offers a serial interface and a software protocol allowing operation on a simple two wire bus with I²C_CLK (SCL of PXA255) and I²C_DATA (SDA of PXA255). The EEPROM is optional and usually not placed.

FIGURE 2.

The slave address of the EEPROM:



- Read address: A1
- Write address: A0

3.4 CompactFlash socket type II

CompactFlash is a very small removable mass storage device. It provides complete PCMCIA-ATA functionality and compatibility plus TrueIDE functionality compatible with ATA/ATAPI-4. At 43mm (1.7“) x 36mm (1.4“) x 3.3mm (0.13“), the device’s thickness is less than one-half of a current PCMCIA Type II card. It is actually one-fourth the volume of a PCMCIA card. Compared to a 68-pin PCMCIA card, a CompactFlash card has 50 pins (the connector is similar to the PCMCIA card) but still conforms to PCMCIA-ATA specs. CompactFlash cards are designed with flash technology, a non-volatile storage solution that does not require a battery to retain data indefinitely. CompactFlash storage products are solid state, meaning they contain no moving parts, and provide users with much greater protection of their data than conventional magnetic disk drives.

The ConXS is delivered with a Type II CompactFlash socket.

TABLE 1.

CF Status Register

| Offset 0x00000000 | | | | | | | | | | | | | | | | CF Status Register | | | |
|-------------------|-----------|----|-----------|--|----|----|---|---|---|---|---|---|---------|---|----------|--------------------|--|--|--|
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | |
| Reserved | | | | | | | | | | | | | VS[1:0] | | BVD[1:0] | | | | |
| Bits | Name | | Type | Description | | | | | | | | | | | | | | | |
| 1:0 | BVD[2..1] | | Read Only | Charge Condition of PC-card 00 - Battery low, data loss 01 - Warning, battery must be changed, but no data loss till now 10 - Battery low, data loss 11 - Battery OK | | | | | | | | | | | | | | | |
| 3:2 | VS[2:1] | | Read Only | Voltage Sense lines 11 - 5V operation (unsupported) 0x - 3V3 operation | | | | | | | | | | | | | | | |

3.5 Board Control Register BCR

The ConXS board requires additional GPIO output functions, which are implemented in the Board Control Register (BCR) to control Compact Flash and display.

TABLE 2.

Board Control Register

| Offset 0x02000000 | | | | | | | | | | Board Control Register | | | | | | |
|-------------------|-----------------|----|------------|--|----|----|---|---|---|------------------------|----------|-----------|--------|----------|----------|------------------|
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | ? | ? | ? | ? | ? | ? | ? | ? | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| Reserved | | | | | | | | | | CF_RESET | Reserved | CF_BUF_EN | L_DISP | Reserved | Reserved | S0_POW_EN [0..1] |
| Bits | Name | | Type | Description | | | | | | | | | | | | |
| 1:0 | S0_POW_EN[1..0] | | Write Only | CompactFlash Power Enable x1, 1x - Power ON 00 - Power OFF | | | | | | | | | | | | |
| 2 | Reserved | | - | - | | | | | | | | | | | | |
| 3 | Reserved | | - | - | | | | | | | | | | | | |
| 4 | L_DISP | | Write Only | Display enable 0 - Display off 1 - Display on | | | | | | | | | | | | |
| 5 | CF_BUF_EN | | Write Only | Compact Flash buffer enable 0 - CF buffer enable ON 1 - CF buffer enable OFF | | | | | | | | | | | | |
| 6 | Reserved | | - | - | | | | | | | | | | | | |
| 7 | CF_RESET | | Write Only | Resetting Compact Flash card 0 - Normal operation 1 - Resetting PCMCIA | | | | | | | | | | | | |

With setting the data bus D04 the display control signal L_DISP can be switched. The important thing about that is the power on/off timing of the display. Usually the correct sequence is as followed:

1. Power Supply
2. Input signal
3. Contrast voltage
4. Display control signal L_DISP

If you use another display as delivered from Keith & Koep you should test the correctness of the power on/off sequences. Resetting the data bus D05 switches the address and control-signals of the CF-buffer.

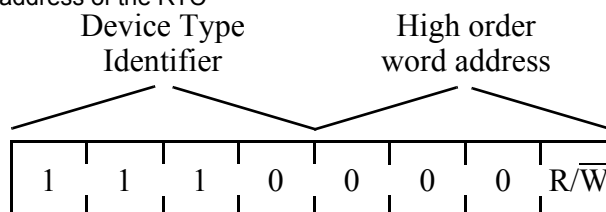
With setting the data bus D07 a reset-signal is sent to the Compact Flash slot.

3.6 Real Time Clock (RTC)

ConXS contains a Low-Power RTC from Philips, called PCF8593. This chip uses the same two wire bus as the serial EEPROM, which is described in figure 2 on page 5.

FIGURE 3.

The slave address of the RTC



Read address: A3

Write address: A2

The RTC is supplied from an external battery.

3.7 Reset

There are two sources of reset on the ConXS:

1. Power-on Reset
2. Reset from the watchdog timer

Power-on reset is generated automatically when power is applied to the board. It can also be initiated by a push button switch attached to a 2-pole 0.1-inch pitch connector on the board.

Resets generated by any of these methods are equivalent and indistinguishable.

3.8 Power Supply

The power supply is done through a 2-pin connector by Phoenix. The input voltage range is from +12V to +24V.

3.9 Power generation on board

The power supplies +5V and +3V3 are generated from the input voltage by two DC-DC converters. The +5V are used for USB, CompactFlash cards and for back-light inverter. The +3V3 are used by Trizeps III / IV, CompactFlash cards, serial interfaces and other components. The +1V8V is generated from +3V3, it is needed as core voltage of the CPLD.

3.10 GPIO

The PXA255 (Trizeps III) processor enables and controls 81 general purpose I/O (GPIO) pins through the use of 27 registers which configure the pin direction (input or output), pin function, pin state (outputs only), pin level detection (inputs only), and selection of alternate functions. The PXA255 processor provides 81 GPIO pins for use in generating and capturing application specific input and output signals. Each pin can be programmed as either an input or output. When programmed to be an input, a GPIO can also serve as an interrupt source. If a GPIO is used for it alter-

nate function it cannot be used as a GPIO at the same time. Table 3 below shows each pin and the use on ConXS. The PXA270 on Trizeps IV provides 118 GPIO pins. They are shown in table 4.

TABLE 3. GPIOs of PXA255 (Trizeps III) used on ConXS base board .

| PXA255 Pin | Function on ConXS | Dir | Description | Pin on SODIMM |
|-------------------|--------------------------------|-----|------------------------------|-----------------------------------|
| GP[80] | $\overline{CS}[4]$ | out | Active low chip select 4 | 106 |
| GP[79] | $\overline{CS}[3]$ | out | Active low chip select 3 | 107 |
| GP[78] | internally used on Trizeps III | - | $\overline{CS}2$ for DM9000 | - |
| GP[77] | L_BIAS | out | LCD AC BIAS | 44 |
| GP[76] | L_PCLK | out | LCD pixel clock | 56 |
| GP[75] | L_LCLK | out | LCD line clock | 68 |
| GP[74] | L_FCLK | out | LCD frame clock | 82 |
| GP[73] | LDD15 | out | LCD data pin 15 | 64 |
| GP[72] | LDD14 | out | LCD data pin 14 | 66 |
| GP[71] | LDD13 | out | LCD data pin 13 | 54 |
| GP[70] | LDD12 | out | LCD data pin 12 | 52 |
| GP[69] | LDD11 | out | LCD data pin 11 | 50 |
| GP[68] | LDD10 | out | LCD data pin 10 | 74 |
| GP[67] | LDD09 | out | LCD data pin 9 | 48 |
| GP[66] | LDD08 | out | LCD data pin 8 | 62 |
| GP[58]- GP[65] | LDD[00-07] | out | LCD data pin 0 to7 | 76, 70, 60, 58, 78, 72, 80, 46 |
| GP[57] | $\overline{PIOIS16}$ | in | Bus Width select I/O card | 104 |
| GP[56] | \overline{PWAIT} | in | Wait signal for card space | 102 |
| GP[55] | \overline{PREG} | out | Card address bit 26 | 98 |
| GP[54] | PSKTSEL | out | Socket select for card space | 100 |
| GP[53] | $\overline{PCE2}$ | out | Card Enable for card space | 96 |
| GP[52] | $\overline{PCE1}$ | out | Card Enable for card space | 94 |
| GP[51] | \overline{PIOW} | out | I/O Write for Card space | 101 |
| GP[50] | \overline{PIOR} | out | I/O Read for Card space | 103 |
| GP[49] | \overline{PWE} | out | Write enable for card space | 99 |
| GP[48] | \overline{POE} | out | Output Enable for card space | 97 |
| GP[47] | TXD_2 | out | STD_UART transmit data | 21 |
| GP[46] | RXD_2 | in | STD_UART receive data | 19 |
| GP[45] | BT_RTS | out | BTUART request to send | 34 |
| GP[44] | BT_CTS | in | BTUART clear to send | 32 |
| GP[43] | BT_TXD | out | BTUART transmit data | 38 |
| GP[42] | BT_RXD | in | BTUART receive data | 36 |
| GP[41] | FF_RTS | out | FFUART request to send | 27 |
| GP[40] | FF_DTR | out | FFUART data terminal ready | 23 |

| PXA255 Pin | Function on ConXS | Dir | Description | Pin on SODIMM |
|------------|--------------------------------|-----|----------------------------|---------------|
| GP[39] | FF_TXD | out | FFUART transmit data | 35 |
| GP[38] | FF_RI | in | FFUART ring indicator | 37 |
| GP[37] | FF_DSR | in | FFUART data set ready | 29 |
| GP[36] | FF_DCD | in | FFUART data carrier detect | 31 |
| GP[35] | FF_CTS | in | FFUART clear to send | 25 |
| GP[34] | FF_RXD | in | FFUART receive data | 33 |
| GP[33] | internally used on Trizeps III | - | Active low chip select 5 | - |
| GP[32] | GPIO32 | | GPIO32 | 73 |
| GP[31] | internally used on Trizeps III | - | AC97 sync | - |
| GP[30] | internally used on Trizeps III | - | AC97 Sdata_out | - |
| GP[29] | internally used on Trizeps III | - | AC97 Sdata_in0 | - |
| GP[28] | internally used on Trizeps III | - | AC97 bit_clk | - |
| GP[27] | RESET_BT | out | Reset signal for Bluetooth | 85 |
| GP[26] | GPIO26 | bi | MMC_DAT1 | 81 |
| GP[25] | PWR_FAIL | in | Powerfail IRQ | 79 |
| GP[24] | $\overline{\text{PCD}}$ | in | PCMCIA card detect | 77 |
| GP[23] | GPIO23 | in | TTL I/O IRQ | 75 |
| GP[22] | internally used on Trizeps III | - | used for USB Slave | - |
| GP[21] | TTLIO_IRQ | in | IRQ TTLIO | 71 |
| GP[20] | $\overline{\text{IRQ_HIL}}$ | in | IRQ Hilscher | 69 |
| GP[19] | internally used on Trizeps III | - | used for DM9000 | - |
| GP[18] | RDY | in | External bus ready | 95 |
| GP[17] | GPIO17 | bi | Extension bus header | 67 |
| GP[16] | GPIO16 | bi | Extension bus header | 65 |
| GP[15] | $\overline{\text{CS1}}$ | out | Active low chip select 1 | 105 |
| GP[14] | GPIO14 | bi | Extension bus header | 63 |
| GP[13] | GPIO13 | bi | Extension bus header | 61 |
| GP[12] | MMC_DET | in | MMC detection | 59 |
| GP[11] | GPIO11 | bi | Extension bus header | 57 |
| GP[10] | IRQ_USB_SL | in | Interrupt USB-Slave | 55 |
| GP[9] | GPIO09 | bi | Extension bus header | 53 |
| GP[8] | MMC_CS0 | out | MMC Chip select 0 | 51 |
| GP[7] | GPIO07 | bi | Extension bus header | 49 |
| GP[6] | MMC_CLK | out | MMC clock | 47 |
| GP[5] | internally used on Trizeps III | - | | - |

| PXA255 Pin | Function on ConXS | Dir | Description | Pin on SODIMM |
|------------|--------------------------------|-----|-------------|---------------|
| GP[4] | internally used on Trizeps III | - | | - |
| GP[3] | internally used on Trizeps III | - | | - |
| GP[2] | internally used on Trizeps III | - | | - |
| GP[1] | PRDY | in | PCMCIA IRQ | 45 |
| GP[0] | IRQ_PIC | in | PIC IRQ | 43 |

TABLE 4.

GPIOs of PXA270 (Trizeps IV)

| PXA270 Pin | Function on ConXS | Dir | Description | Pin on SODIMM |
|------------|-------------------------------|-----|-----------------------------------|---------------|
| GP[118] | I2C_DATA | bi | I2C data signal | 194 |
| GP[117] | $\overline{\text{I2C_CLK}}$ | out | I2C clock signal | 196 |
| GP[116] | CIF_DD2 | in | camera data signal s | 57 |
| GP[115] | not connected | | | - |
| GP[114] | CIF_DD1 | in | camera data | 53 |
| GP[113] | internally used on Trizeps IV | | | - |
| GP[112] | MMCCMD | bi | command line | 190 |
| GP[111] | MMCDAT3 | bi | multimedia card data | 51 |
| GP[110] | MMCDAT2 | bi | multimedia card data | 85 |
| GP[109] | MMCDAT1 | bi | multimedia card data | 81 |
| GP[108] | CIF_DD7 | in | camera data signal | 71 |
| GP[107] | CIF_DD8 | in | camera data signal | 73 |
| GP[106] | CIF_DD9 | in | camera data signal | 75 |
| GP[105] | internally used on Trizeps IV | | IRQ_USB_SL (USB 5V present) | - |
| GP[104] | PSKTSEL | out | Socket select for card space | 100 |
| GP[103] | CIF_DD3 | in | camera data signal | 61 |
| GP[102] | $\overline{\text{PCE1}}$ | out | Card enable for card space | 94 |
| GP[101] | internally used on Trizeps IV | | IRQ_DAVICOM Ethernet | - |
| GP[100] | internally used on Trizeps IV | | DREQ2 | - |
| GP[99] | not used | | | - |
| GP[98] | not used | | | - |
| GP[97] | internally used on Trizeps IV | | DAVICOM_WAKEUP | - |
| GP[96] | FF_RDX | in | FFUART receive data | 33 |
| GP[95] | internally used on Trizeps IV | out | $\overline{\text{USB_OTG_RST}}$ | - |

TABLE 4. GPIOs of PXA270 (Trizeps IV)

| PXA270 Pin | Function on ConXS | Dir | Description | Pin on SODIMM |
|------------|--------------------------------|-----|----------------------------|---------------|
| GP[94] | internally used on Trizeps IV | out | LOCK_DiskOnChip | - |
| GP[93] | internally used on Trizeps IV | in | IRQ_DiskOnChip | - |
| GP[92] | MMCDAT0 | bi | multimedia card data | 192 |
| GP[91] | CIF_DD5/UCLK | bi | camera data signal | 65 |
| GP[90] | CIF_DD4 | bi | camera data signal | 63 |
| GP[89] | USBHPEN1 | | | 129 |
| GP[88] | USBHPWR1 | | | 131 |
| GP[87] | not used | out | LCD data pin 17 | - |
| GP[86] | not used | out | LCD data pin 16 | - |
| GP[85] | GP85_IRQ_HIL | | | 69 |
| GP[84] | not used | | | - |
| GP[83] | FF_RTS | out | FFUART request to send | 27 |
| GP[82] | FF_DTR | out | FFUART data terminal ready | 23 |
| GP[81] | POWERFAIL | in | POWERFAIL IRQ | 79 |
| GP[80] | $\overline{CS[4]}$ | out | Active low chip select 4 | 106 |
| GP[79] | $\overline{CS[3]}$ | out | Active low chip select 3 | 107 |
| GP[78] | internally used on Trizeps III | out | $\overline{CS2_DM9000}$ | - |
| GP[77] | L_BIAS | out | LCD AC BIAS | 44 |
| GP[76] | L_PCLK | out | LCD pixel clock | 56 |
| GP[75] | L_LCLK | out | LCD line clock | 68 |
| GP[74] | L_FCLK | out | LCD frame clock | 82 |
| GP[73] | LDD15 | out | LCD data pin 15 | 64 |
| GP[72] | LDD14 | out | LCD data pin 14 | 66 |
| GP[71] | LDD13 | out | LCD data pin 13 | 54 |
| GP[70] | LDD12 | out | LCD data pin 12 | 52 |
| GP[69] | LDD11 | out | LCD data pin 11 | 50 |
| GP[68] | LDD10 | out | LCD data pin 10 | 74 |
| GP[67] | LDD09 | out | LCD data pin 09 | 48 |
| GP[66] | LDD08 | out | LCD data pin 08 | 62 |
| GP[65] | LDD07 | out | LCD data pin 07 | 46 |
| GP[64] | LDD06 | out | LCD data pin 06 | 80 |
| GP[63] | LDD05 | out | LCD data pin 05 | 72 |
| GP[62] | LDD04 | out | LCD data pin 04 | 78 |
| GP[61] | LDD03 | out | LCD data pin 03 | 58 |
| GP[60] | LDD02 | out | LCD data pin 02 | 60 |

TABLE 4. GPIOs of PXA270 (Trizeps IV)

| PXA270 Pin | Function on ConXS | Dir | Description | Pin on SODIMM |
|------------|-------------------------------|-----|--|---------------|
| GP[59] | LDD01 | out | LCD data pin 01 | 70 |
| GP[58] | LDD00 | out | LCD data pin 00 | 76 |
| GP[57] | $\overline{\text{PIOIS16}}$ | in | Bus width select I/O card | 104 |
| GP[56] | $\overline{\text{PWAIT}}$ | in | Wait signal for card space | 102 |
| GP[55] | $\overline{\text{PREG}}$ | out | Card address bit 26 | 98 |
| GP[54] | $\overline{\text{PCE2}}$ | out | Card enable for card space | 96 |
| GP[53] | not used | | USB_P2_3 | - |
| GP[52] | not used | | UDET | - |
| GP[51] | $\overline{\text{PIOW}}$ | out | I/O write for card space | 101 |
| GP[50] | $\overline{\text{PIOR}}$ | out | I/O read for card space | 103 |
| GP[49] | $\overline{\text{PWE}}$ | out | Write enable for card space | 99 |
| GP[48] | $\overline{\text{POE}}$ | out | Output enable for card space | 97 |
| GP[47] | TXD_2 | out | STD_UART transmit data | 21 |
| GP[46] | RXD_2 | in | STD_UART receive data | 19 |
| GP[45] | BT_RTS | out | BTUART request to send | 34 |
| GP[44] | BT_CTS | in | BTUART clear to send | 32 |
| GP[43] | BT_TXD | out | BTUART transmit data | 38 |
| GP[42] | BT_RXD | in | BTUART receive data | 36 |
| GP[41] | not used | | USB_P2_7 | - |
| GP[40] | not used | | USB_P2_5 | - |
| GP[39] | USB_P2_6 | out | USB speed select (internal) | - |
| GP[38] | FF_RI | in | FFUART ring indicator | 37 |
| GP[37] | USB_P2_8 | out | USB suspend (internal) | - |
| GP[36] | USB_P2_4 | in | USB SE0/VM (internal) | - |
| GP[35] | USB_P2_1 | in | USB $\overline{\text{INT}}$ (internal) | - |
| GP[34] | USB_P2_2 | bi | $\overline{\text{OE/INT}}$ (internal) | - |
| GP[33] | FF_DSR | in | FFUART data set ready | 29 |
| GP[32] | MMCCLK | out | MMC clock | 47 |
| GP[31] | internally used on Trizeps IV | | AC97_SYNC | - |
| GP[30] | internally used on Trizeps IV | out | AC97_DATAOUT | - |
| GP[29] | internally used on Trizeps IV | in | AC97_DATAIN | - |
| GP[28] | internally used on Trizeps IV | out | Bitclock | - |
| GP[27] | CIF_DD0 | in | Camera data signal | 49 |
| GP[26] | CIF_PCLK | in | Camera pixelclock | 90 |
| GP[25] | CIF_LV | in | Camera line clock | 92 |

TABLE 4. GPIOs of PXA270 (Trizeps IV)

| PXA270 Pin | Function on ConXS | Dir | Description | Pin on SODIMM |
|------------|-------------------------------|-----|---|---------------|
| GP[24] | CIF_FV | in | Camera frame clock | 86 |
| GP[23] | CIF_MCLK | out | Camera masterclock | 88 |
| GP[22] | internally used on Trizeps IV | - | GPIO22 | - |
| GP[21] | not used | | $\overline{\text{SDCS3}}$ | - |
| GP[20] | not used | | $\overline{\text{SDCS2}}$ | - |
| GP[19] | not used | | L_CS/URST | - |
| GP[18] | internally used on Trizeps IV | | used for DM9000 | - |
| GP[17] | CIF_DD6 | in | Camera data signal | 67 |
| GP[16] | FF_TXD | out | UART transceive | 35 |
| GP[15] | $\overline{\text{CS1}}$ | out | Active low chip select 1 | 105 |
| GP[14] | not used | | L_VSYNV/UCLK | - |
| GP[13] | GPIO01_PRDY | | | 45 |
| GP[12] | MMCDDET | in | MMC detection | 59 |
| GP[11] | PCD | in | PCMCIA card detect | 77 |
| GP[10] | FF_DCD | in | UART data carrier detect | 31 |
| GP[09] | FF_CTS | in | UART clear to send | 25 |
| GP[8] | PWR_CAP | in | capacitor input | - |
| GP[7] | PWR_CAP | in | capacitor input | - |
| GP[6] | PWR_CAP | in | capacitor input | - |
| GP[5] | PWR_CAP | in | capacitor input | - |
| GP[4] | internally used on Trizeps IV | - | PWR_SDA | - |
| GP[3] | internally used on Trizeps IV | | PWR_SCL | - |
| GP[2] | not available | | system enable | - |
| GP[1] | internally used on Trizeps IV | | IRQ_CODEC | - |
| GP[0] | IRQ_PIC | in | PIC interrupt (ext. i ² c Dev) | 43 |

3.11 Ethernet

The Ethernet Controller on Trizeps III / IV board (DM9000 by Davicom) provides 10 / 100MBit interface

3.12 UART serial ports

The ConXS provides four kinds of serial ports:

- USB
- Bluetooth
- RS232 Standard

- RS232 Full Function
- Network SSP

3.12.1 USB Device Controller - UART

The universal serial bus device controller (UDC) supports three endpoints and can operate half-duplex at a baud rate of 12 Mbps (slave only, not a host or hub controller). The UDC is USB-compliant and supports all standard device requests issued by the host. The external pins dedicated to this interface are UDC+ and UDC-. The USB protocol uses differential signalling between the two pins for half-duplex data transmission. A 1.5 KOhm resistor is connected between GPIO22 and the USB cable's D+ signal to pull the UDC+ pin high when not driven. This signifies the UDC is a high-speed, 12 Mbps device and provides the correct polarity for data transmission.

The UDC is accessible by an USB-B connector. However, the user should refer to the Universal Serial Bus Specification, Revision 1.0¹ for a full description of the USB protocol and its operation.

3.12.2 Bluetooth - UART

The Bluetooth UART is either used with a Bluetooth module (WML-C20AB or WML-C10 on the bottom side of the ConXS) or it is configured as an universal asynchronous receiver / transmitter (UART) serial controller. A Maxim MAX3223 RS232 transceiver is used to manage the level conversion and line interface. The device has a power saving automatic shutdown that powers down the chip if no valid RS232 levels are detected. The component may also be forced off by the FORCEON signal. The Bluetooth UART is accessible by connector J18 (10-pin header). The external pins dedicated to this interface are TXD1, RXD1, RTS1 and CTS1.

For the communication between the PC (DB9 male) and the ConXS a serial extension cable is needed. Therefore the serial port J18 (10 pin header) is to be connected with a short flat cable to a DB9 female connector (see figure 7 on page 40).

3.12.3 Standard UART

The STUART can be used as an IrDA interface. The infrared communications port (ICP) operates at half-duplex and provides direct connection to commercially available Infrared Data Association (IrDA) compliant LED transceivers. The ICP supports both the original IrDA standard with speeds up to 115.2 Kbps as well as the newer 4-Mbps standard. Both standards use different bit encoding techniques and serial packet formats. Low-speed IrDA transmission uses the Hewlett-Packard Serial Infrared standard (HP-SIR) for bit encoding and an UART as the serial engine; high-speed uses Four-Position Pulse Modulation (4PPM) and a specialized serial packet protocol developed expressly for IrDA transmission. Standard UART is accessible by connector J20 (10-pin header). The external pins dedicated to the ICP are TXD2 and RXD2, IRDA_MODE and IRDA_SD are connected to the CPLD.

1. The latest revision of the Universal Serial Bus Specification Revision 1.0 can be accessed via the World Wide Web Internet side at: <http://www.teleport.com/~usb/>

FIGURE 4. Sample: Use of IrDA

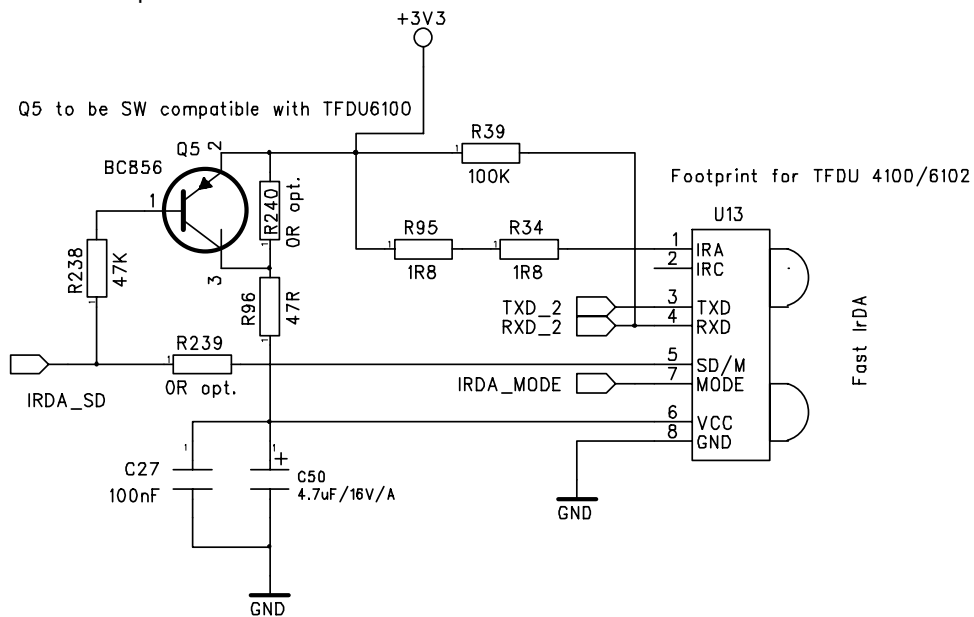


TABLE 5. IrDA Control Register

| Offset 0x02400000 | | | | | | | | | | | | | | IrDA Control Register | | |
|-------------------|-----------|----|------------|---|----|----|---|---|---|---|---|---|---|-----------------------|-----------|---------|
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | 0 | 1 |
| Reserved | | | | | | | | | | | | | | | IRDA_MODE | IRDA_SD |
| Bits | Name | | Type | Description | | | | | | | | | | | | |
| 0 | IRDA_SD | | Write Only | IrDA Shutdown 0 - IrDA activ 1 - IrDA inactiv | | | | | | | | | | | | |
| 1 | IRDA_MODE | | Write Only | IrDA Mode 0 - Low speed 1 - High speed | | | | | | | | | | | | |

Alternately you can use serial port 2 as an UART.

3.12.4 Full Function UART

A Maxim MAX3243 RS232 transceiver is used to manage the level conversion and line interface. The device has a power saving automatic shutdown that powers down the chip if no valid RS232 levels are detected. The component may also be forced off by the FORCEON signal. Full Function UART is accessible by the male serial port connector J5 (DSUB9M). This port provides RTS, CTS, DSR, DTR, DCD and RI modem signals to support a serial IO port PC synchronous application.

3.12.5 Network SSP Serial Port

The NSSP is a synchronous serial interface that connects to a variety of external analog-to-digital (A/D) converters, telecommunication CODECs, and many other devices that use serial protocols for data transfer. The NSSP provides support for the following protocols:

- Texas Instruments (TI) Synchronous Serial Protocol
- Motorola Serial Peripheral Interface (SPI) protocol
- National Semiconductor Microwire
- Programmable Serial Protocol (PSP)

The NSSP operates as full-duplex devices for the TI Synchronous Serial Protocol, SPI, and PSP protocols and as a half-duplex devices for the Microwire devices.

The external pins dedicated to this interface are NSSPTXD, NSSPRXD, NSSPCLK and NSSPFRM. The NSSP is accessible by the extension connector J2.

3.13 TTL I/O

ConXS offers 8 TTL Inputs and 8 TTL Outputs. The TTL Outputs are accessible by the connector J1, the TTL Inputs by the connector J2. The output signals (OUTPUT[0:7]) correspond with dataline signals D[0:7], which are switched by a CPLD. They will be selected by addressing 0x0D800000 (\CS_IO_OUT and \CS_IO_IN). The Inputs can be read as follows:

```
read = *(short *) ADR
```

The Outputs can be written as follows:

```
*(short *) portadr = value
```

3.14 Audio In/Out

The Trizeps III / IV board includes a single chip integrated mixed signal audio and telecom codec (Philips UCB 1400). JJ2 and JJ3 on the ConXS give access to the speaker and microphone signals. The pinout of JJ2 is shown in table 24 on page 42 and of JJ3 in table 25 on page 42.

The ConXS is additionally fitted out with 3.5mm jack chassis sockets for stereo headphone and microphone.

3.15 Display connector, 4 wire Touch Panel, contrast EEPOT and backlight switch

The XScale PXA255/PXA270 on Trizeps III / IV offers a 16 bit LCD-controller. The audio and telecom codec (see chapter 3.14, "Audio In/Out" on page 17) pro-

vides also a 4 wire touch screen interface. The relevant signals are accessible at J14 see table 19 on page 38.

The backlight voltage can be switched by the L_DISP signal (CPLD, see BCR). The backlight voltage can either be switched to input voltage or to +5V. This depends of the inverter type.

The contrast voltage can be adjusted by an Digitally-Controlled Potentiometer by Xicor. The device consists of a resistor array, wiper switches, a control section, and nonvolatile memory. The wiper position is controlled by a three-wire interface.

The potentiometer is implemented by a resistor array composed of 99 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the CS, U/D, and INC inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

TABLE 6.

Display Contrast Register

| Offset 0x03800000 | | | | | | | | | | | Display Contrast Register | | | | | |
|-------------------|-----------|----|------------|--|----|----|---|---|---|---|---------------------------|---|-----------|-----------|----------|---|
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | 1 | 1 |
| Reserved | | | | | | | | | | | | | EEPOT_U_D | EEPOT_INC | EEPOT_CS | |
| | | | | | | | | | | | | | | | | |
| Bits | Name | | Type | Description | | | | | | | | | | | | |
| 0 | EEPOT_CS | | Write Only | Chip Select of EEPROM 0 - activ 1 - inactiv | | | | | | | | | | | | |
| 1 | EEPOT_INC | | Write Only | Increment of EEPROM 0 - increment by 1 1 - inactive | | | | | | | | | | | | |
| 2 | EEPOT_U_D | | Write Only | Direction (Up/Down)of EEPROM 0 - decrement 1 - increment | | | | | | | | | | | | |

All of these signals are available at the 40-pin connector J14 (description: table 19 on page 38).

3.16 SD / MMC connector

The MultiMediaCard standard grew out of a joint development between SanDisk Corporation and Siemens AG/Infineon Technologies AG, and was introduced in November 1997. MultiMediaCards weigh less than two grams and, about the size of a postage stamp, are the world’s smallest (24mm x 32mm x 1.4 mm) removable solid-state memory solutions for mobile applications. These convenient, reliable, rugged and lightweight standardized data carriers store up to 64 MBytes.

MultiMediaCards use ROM technology for read-only applications and Flash technology for read/write applications. The cards are fast for excellent system performance; energy efficient for prolonged battery life in portable products; and cost-

efficient for use in systems sold at consumer price points. The simple molded package has a seven pad (pin) serial interface. This easy-to-install simple serial interface offers easy integration into various devices regardless of the microprocessor used. The MultiMediaCard has a wide variety of uses in some of the most exciting products on the market today.

The socket is on the top side (J25).

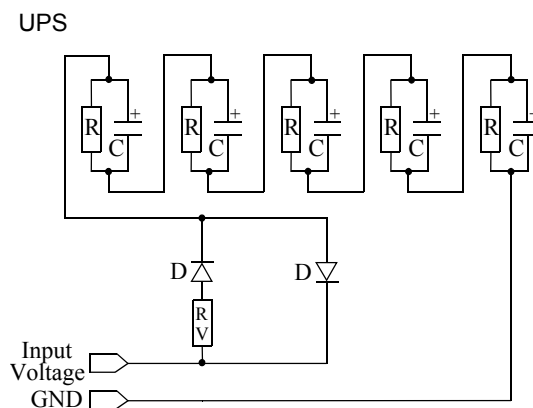
3.17 Powerfail - Interrupt

Falling down power supply under $\sim 8V$ generates an interrupt GPIO25 (Powerfail-IRQ).

3.18 Uninterruptible Power Supply (UPS)

The easiest way to get an UPS is to use the following electrical circuit.

FIGURE 5.



Values:
 R: $22K\Omega$
 RV: 10Ω (Power resistor)
 C: $10F / 2,3V$ (UltraCap by EPCOS)
 D: 1N5819

You can use connector J23 to supply this circuit with Input voltage and Ground.

Attention: To avoid damage of UltraCap the Input Voltage should be smaller than 12V

This circuit is able to supply the ConXS with Trizeps III in case of Powerfail for about 15 seconds.

TABLE 7.

UPS Register

| Offset 0x02800000 | | | | | | | | | | | UPS Register | | | | | |
|-------------------|---------------|----|-----------------|--|----|----|---|---|---|---|--------------|------------|---------------|--------------|--------|---------|
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | 0 | 1 | 1 | 0 | 0 |
| Reserved | | | | | | | | | | | | BATT_EMPTY | AUTO_DSPL_OFF | AUTO_PWR_OFF | CHARGE | BATT_EN |
| Bits | Name | | Type | Description | | | | | | | | | | | | |
| 0 | BATT_EN | | Output R/W | External battery enable signal 0 - external battery OFF 1 - external battery ON | | | | | | | | | | | | |
| 1 | CHARGE | | Output R/W | Charge external battery 0 - Do not charge 1 - Charge | | | | | | | | | | | | |
| 2 | AUTO_PWR_OFF | | Flag R/W | Turn off system flag 0 - OS does not power down after powerfail-IRQ 1 - OS powers down after powerfail-IRQ | | | | | | | | | | | | |
| 3 | AUTO_DSPL_OFF | | Flag R/W | Turn off backlight inverter flag 0 - Leave backlight ON 1 - Powerfail-IRQ handler switches backlight OFF | | | | | | | | | | | | |
| 4 | BATT_EMPTY | | Input Read Only | External battery status 0 - External battery empty 1 - External battery full | | | | | | | | | | | | |

3.19 USB Host connector

The Trizeps III is featured by Transdimension’s high performance embedded USB host/slave controller. This controller is capable of the USB 2.0 OTG protocol and has a maximal Bitrate of 12MB. The chip is optimized to generate minimal CPU overhead.

ConXS offers a double USB A connector (J12) to connect mouse, keyboard, memory cards or others. Alternately you can use one of this ports to get USB OTG by an 5-pin Header (J21)

3.20 NV-SRAM

ConXS can be fitted out with a Non-Volatile SRAM K6X4016T3F by Samsung. It is a Low Power and Low Voltage CMOS Static RAM organized as 256Kx16 bit. The SRAM is optional and usually not placed. The SRAM is supplied from an external battery.

3.21 Hilscher COM-Module connector

ConXS offers an 50-pin high density connector for Hilscher-COM modules. You can find the pin description on table 11 on page 32.

3.22 Extension bus connector

Con XS offers a second 50-pin high density connector as extension bus. You can find the pin description on table 12 on page 34.

Appendix A

In this chapter you can find detailed description about all headers and connectors on ConXS.

A.1 Overview of all jumpers, connectors

TABLE 8.

Overview of all jumpers and connectors

| Name | Function | Type |
|------|--|----------------------------------|
| M16 | Trizeps III /IV connector | |
| J1 | Hilscher COM-Module connector | Samtec FTSH-125-01-LDV |
| J2 | Extension bus connector | Samtec FTSH-125-01-LDV |
| J3 | Uninterruptible Power Supply (UPS) connector | Header SL2-10 |
| J4 | JTAG connector (CPLD) | Header SL2-6 |
| J5 | RS232 connector (port 3) | DSUB9 male |
| J7 | Power Supply | Phoenix MSTBA2,5/2-G-5.08 |
| J8 | Ethernet RJ45 connector | HFJ11-2450E-L12 |
| J12 | USB-A connector | AMP 787617-x |
| J14 | Display connector | Header SL2-40 |
| J18 | RS232 connector (port 1) | Header SL2-10 |
| J20 | IrDA connector / DIAG Hilscher | Header SL2-10 |
| J21 | USB Mini-AB (OTG) | Header SL1-5 |
| J22 | USB-B connector | Reichelt USB PCB BW |
| J25 | SD / MMC card connector | Yamaichi Electronics FPS009-2405 |
| JJ2 | Speaker connector | Header SL1-2 |
| JJ3 | Microphone connector | Header SL1-2 |
| JJ4 | Backlight power select connector | Header SL1-3 |
| JJ5 | Reset connector | Header SL1-2 |
| JJ6 | Code select CPLD connector | Header SL1-2 |
| JJ8 | Angelboot connector | Header SL1-2 |
| U1 | Headphone connector | JISC 150301 |
| U7 | Compact Flash connector (bottom side) | 3M N7E50-7516-xx |
| U14 | Microphone connector | JISC 150301 |

A.2 Trizeps III Connector M16

In the following you find the pinout of the Trizeps III socket.

TABLE 9.

M16 - Trizeps III connector

| Pin | Name | Description |
|-----|---------------|--|
| 1 | MIC_OUT | microphone input signal |
| 2 | AD3 | analog voltage input (UCB 1400) |
| 3 | MIC_GND | microphone ground switch input |
| 4 | VIN_AD2 | analog voltage input (UCB 1400) ^a |
| 5 | LINEIN_L | Line in left channel (UCB1400) |
| 6 | AD1 | analog voltage input (UCB 1400) |
| 7 | LINEIN_R | Line in right channel (UCB1400) |
| 8 | VBAT_AD0 | analog voltage input (UCB 1400) |
| 9 | VSSA_AUDIO | Analog ground audio (UCB 1400) |
| 10 | VDDA_AUDIO | Analog power audio (UCB 1400) |
| 11 | VSSA_AUDIO | Analog ground audio (UCB 1400) |
| 12 | VDDA_AUDIO | Analog power audio (UCB 1400) |
| 13 | HEADPHONE_GND | Line out ground output (UCB 1400) |
| 14 | TSPX | positive X-plate touch screen (UCB 1200) |
| 15 | HEADPHONE_L | Line out left channel (UCB1400) |
| 16 | TSMX | negative X-plate touch screen (UCB 1200) |
| 17 | HEAPHONE_R | Line out right channel (UCB 1400) |
| 18 | TSPY | positive Y-plate touch screen (UCB 1200) |
| 19 | RXD_2 | serial port two receive pin (IrDA) (PXA 255) |
| 20 | TSMY | negative Y-plate touch screen (UCB 1200) |
| 21 | TXD_2 | serial port two transmit pin (IrDA) (PXA 255) |
| 22 | VDD_FAULT | not used |
| 23 | FF_DTR | Full Function UART Data Terminal Ready |
| 24 | BATT_FAULT | not used |
| 25 | FF_CTS | Full Function UART Clear To Send |
| 26 | RESET_IN | reset input |
| 27 | FF_RTS | Full Function UART Ready To Send |
| 28 | TUDC- | serial port zero bidirectional (UDC) (PXA 255) |
| 29 | FF_DSR | Full Function UART Data Set Ready |
| 30 | TUDC+ | serial port zero bidirectional (UDC) (PXA 255) |
| 31 | FF_DCD | Full Function UART Data Carrier Detect |
| 32 | BT_CTS | BlueTooth UART Clear To Send |
| 33 | FF_RXD | Full Function UART Receive Data |
| 34 | BT_RTS | BlueTooth UART Ready To Send |

TABLE 9.

M16 - Trizeps III connector

| Pin | Name | Description |
|-----|-------------------|---------------------------------------|
| 35 | FF_TXD | Full Function UART Transmit Data |
| 36 | BT_RXD | BlueTooth UART Receive Data |
| 37 | FF_RI | Full Function UART Ring Indicator |
| 38 | BT_TXD | BlueTooth UART Transmit Data |
| 39 | GND | Ground |
| 40 | +3V3 | Power Supply |
| 41 | GND | Ground |
| 42 | +3V3 | Power Supply |
| 43 | GPIO00_IRQ_PIC | General purpose I/O |
| 44 | L_BIAS | LCD controller display data (PXA 255) |
| 45 | GPIO01_PRDY | General purpose I/O |
| 46 | LDD07 | LCD controller display data (PXA 255) |
| 47 | GPIO06_MMC_CLK | General purpose I/O |
| 48 | LDD09 | LCD controller display data (PXA 255) |
| 49 | GPIO07 | General purpose I/O |
| 50 | LDD11 | LCD controller display data (PXA 255) |
| 51 | MMC_DAT3 | Multimedia Card data signal D3 |
| 52 | LDD12 | LCD controller display data (PXA 255) |
| 53 | GPIO09 | General purpose I/O |
| 54 | LDD13 | LCD controller display data (PXA 255) |
| 55 | GPIO10_IRQ_USB_SL | General purpose I/O |
| 56 | L_PCLK | LCD pixel clock (PXA 255) |
| 57 | GPIO11 | General purpose I/O |
| 58 | LDD03 | LCD controller display data (PXA 255) |
| 59 | GPIO12_MMC_DET | General purpose I/O |
| 60 | LDD02 | LCD controller display data (PXA 255) |
| 61 | GPIO13 | General purpose I/O |
| 62 | LDD08 | LCD controller display data (PXA 255) |
| 63 | GPIO14 | General purpose I/O |
| 64 | LDD15 | LCD controller display data (PXA 255) |
| 65 | GPIO16 | General purpose I/O |
| 66 | LDD14 | LCD controller display data (PXA 255) |
| 67 | GPIO17 | General purpose I/O |
| 68 | L_LCLK | LCD line clock (PXA 255) |
| 69 | GPIO20/IRQ_HIL | General purpose I/O |
| 70 | LDD01 | LCD controller display data (PXA 255) |
| 71 | GPIO21_TTLIO_IRQ | General purpose I/O |
| 72 | LDD05 | LCD controller display data (PXA 255) |
| 73 | GPIO32 | General purpose I/O |

TABLE 9.

M16 - Trizeps III connector

| Pin | Name | Description |
|-----|----------------------------------|--|
| 74 | LDD10 | LCD controller display data (PXA 255) |
| 75 | GPIO23 | General purpose I/O |
| 76 | LDD00 | LCD controller display data (PXA 255) |
| 77 | GPIO24_ $\overline{\text{PCD}}$ | General purpose I/O |
| 78 | LDD04 | LCD controller display data (PXA 255) |
| 79 | GPIO25_POWERFAIL | General purpose I/O |
| 80 | LDD06 | LCD controller display data (PXA 255) |
| 81 | MMC_DAT1 | Multimedia Card data signal D1 |
| 82 | L_FCLK | LCD frame clock (PXA 255) |
| 83 | GND | Ground |
| 84 | +3V3 | Power Supply |
| 85 | MMC_DAT2 | Multimedia Card data signal D2 |
| 86 | NSSPFRM | Network Synchronous Serial port frame (PXA 255) |
| 87 | $\overline{\text{RESET_OUT}}$ | Reset output (PXA 255) |
| 88 | NSSPCLK | Network Synchronous Serial port clock |
| 89 | $\overline{\text{WE}}$ | Memory Write Enable (PXA 255) |
| 90 | NSSPRXD | Network Synchronous Serial port receive |
| 91 | $\overline{\text{OE}}$ | Memory Output Enable (PXA 255) |
| 92 | NSSPTXD | Network Synchronous Serial port transmit |
| 93 | $\text{RD}/\overline{\text{WR}}$ | read/write direction control for memory bus (PXA255) |
| 94 | $\overline{\text{PCE1}}$ | PCMCIA card enable (low-byte lane) (PXA 255) |
| 95 | GPIO18/ $\overline{\text{RDY}}$ | not used |
| 96 | $\overline{\text{PCE2}}$ | PCMCIA card enable (high-byte lane) (PXA 255) |
| 97 | $\overline{\text{POE}}$ | PCMCIA output enable (PXA 255) |
| 98 | $\overline{\text{PREG}}$ | PCMCIA register select (PXA 255) |
| 99 | $\overline{\text{PWE}}$ | PCMCIA write enable (PXA 255) |
| 100 | PSKTSEL | PCMCIA socket select (PXA 255) |
| 101 | $\overline{\text{PIOW}}$ | PCMCIA I/O write (PXA 255) |
| 102 | $\overline{\text{PWAIT}}$ | PCMCIA wait (PXA 255) |
| 103 | $\overline{\text{PIOR}}$ | PCMCIA I/O read (PXA 255) |
| 104 | $\overline{\text{PIOIS16}}$ | I/O select 16 (PXA 255) |
| 105 | $\overline{\text{CS1}}$ | static chip select (PXA 255) |
| 106 | $\overline{\text{CS4}}$ | static chip select (PXA 255) |
| 107 | $\overline{\text{CS3}}$ | static chip select (PXA 255) |
| 108 | +3V3 | Power Supply |
| 109 | GND | Ground |
| 110 | A08 | memory address bus (PXA 255) |
| 111 | A00 | memory address bus (PXA 255) |

TABLE 9.

M16 - Trizeps III connector

| Pin | Name | Description |
|-----|---------------------------------|---|
| 112 | A09 | memory address bus (PXA 255) |
| 113 | A01 | memory address bus (PXA 255) |
| 114 | A10 | memory address bus (PXA 255) |
| 115 | A02 | memory address bus (PXA 255) |
| 116 | A11 | memory address bus (PXA 255) |
| 117 | A03 | memory address bus (PXA 255) |
| 118 | A12 | memory address bus (PXA 255) |
| 119 | A04 | memory address bus (PXA 255) |
| 120 | A13 | memory address bus (PXA 255) |
| 121 | A05 | memory address bus (PXA 255) |
| 122 | A14 | memory address bus (PXA 255) |
| 123 | A06 | memory address bus (PXA 255) |
| 124 | A15 | memory address bus (PXA 255) |
| 125 | A07 | memory address bus (PXA 255) |
| 126 | DQM0 | not used |
| 127 | $\overline{\text{OTG_EXTVB0}}$ | Turn on/off the external Vbus for OTG operation |
| 128 | DQM1 | not used |
| 129 | $\overline{\text{OTG_PO}}$ | Turn on/off the gang power for all host ports |
| 130 | DQM2 | not used |
| 131 | $\overline{\text{OTG_OC}}$ | Over current condition indicator for gang powered host ports |
| 132 | DQM3 | not used |
| 133 | OTG_VBP | Vbus pulsing control |
| 134 | A25 | memory address bus (PXA 255) |
| 135 | OTG_VBUS | Vbus input sampled during HNP/SRPOperations by the OTG port |
| 136 | A24 | memory address bus (PXA 255) |
| 137 | OTG_ID | Connected to the ID-pin of the Mini-AB connector for OTG applications |
| 138 | A23 | memory address bus (PXA 255) |
| 139 | OTG_DP2 | Data line for Port 2 |
| 140 | A22 | memory address bus (PXA 255) |
| 141 | OTG_DM2 | Data line for Port 2 |
| 142 | A21 | memory address bus (PXA 255) |
| 143 | OTG_DP1 | Data line for Port 1 |
| 144 | A20 | not used |
| 145 | OTG_DM1 | Data line for Port 1 |
| 146 | A19 | not used |
| 147 | GND | Ground |
| 148 | +3V3 | Power Supply |

TABLE 9.

M16 - Trizeps III connector

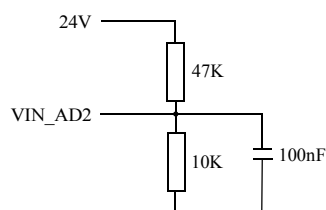
| Pin | Name | Description |
|-----|------------------------------------|------------------------------|
| 149 | D00 | memory data (PXA 255) |
| 150 | D16 | not used |
| 151 | D01 | memory data (PXA 255) |
| 152 | D17 | not used |
| 153 | D02 | memory data (PXA 255) |
| 154 | D18 | not used |
| 155 | D03 | memory data (PXA 255) |
| 156 | D19 | not used |
| 157 | D04 | memory data (PXA 255) |
| 158 | D20 | not used |
| 159 | D05 | memory data (PXA 255) |
| 160 | D21 | not used |
| 161 | D06 | memory data (PXA 255) |
| 162 | D22 | not used |
| 163 | D07 | memory data (PXA 255) |
| 164 | D23 | not used |
| 165 | D08 | memory data (PXA 255) |
| 166 | D24 | not used |
| 167 | D09 | memory data (PXA 255) |
| 168 | D25 | not used |
| 169 | D10 | memory data (PXA 255) |
| 170 | D26 | not used |
| 171 | D11 | memory data (PXA 255) |
| 172 | D27 | not used |
| 173 | D12 | memory data (PXA 255) |
| 174 | D28 | not used |
| 175 | D13 | memory data (PXA 255) |
| 176 | D29 | not used |
| 177 | D14 | memory data (PXA 255) |
| 178 | D30 | not used |
| 179 | D15 | memory data (PXA 255) |
| 180 | D31 | not used |
| 181 | GND | Ground |
| 182 | +3V3 | Power Supply |
| 183 | $\overline{\text{ETH_LINK_AKT}}$ | Link LED signal |
| 184 | A18 | memory address bus (PXA 255) |
| 185 | $\overline{\text{ETH_SPEED100}}$ | Speed LED signal |
| 186 | A17 | memory address bus (PXA 255) |
| 187 | ETH_TX0- | TP TX Output |

TABLE 9.

M16 - Trizeps III connector

| Pin | Name | Description |
|-----|-----------------|--------------------------------|
| 188 | A16 | memory adress bus (PXA 255) |
| 189 | ETH_TX0+ | TP TX Output |
| 190 | MMC_CMD | MultiMedia card command |
| 191 | ETH_AGND | Analog Ground |
| 192 | MMC_DAT | Multimedia Card data signal D0 |
| 193 | ETH_RXI- | TP RX Input |
| 194 | I2C_DATA | I ² C bus data |
| 195 | ETH_RXI+ | TP RX Input |
| 196 | I2C_CLK/ANGBOOT | I ² C bus clock |
| 197 | GND | Ground |
| 198 | +3V3 | Power Supply |
| 199 | GND | Ground |
| 200 | +3V3 | Power Supply |

a. For an input voltage of 24V VIN_AD2 is about 4.21V



A.3 Trizeps IV Connector M16

The pin assignment of the Trizeps IV module is the same as on Trizeps III except the functions of the signals shown in table 10.

TABLE 10.

| Pin | Name | Description |
|-----|---------|--------------------|
| 49 | CIF_DD0 | Camera data signal |
| 53 | CIF_DD1 | Camera data signal |
| 57 | CIF_DD2 | Camera data signal |
| 61 | CIF_DD3 | Camera data signal |

TABLE 10.

| Pin | Name | Description |
|-----|---------------|----------------------------|
| 63 | CIF_DD4 | Camera data signal |
| 65 | CIF_DD5 | Camera data signal |
| 67 | CIF_DD6 | Camera data signal |
| 71 | CIF_DD7 | Camera data signal |
| 73 | CIF_DD8 | Camera data signal |
| 75 | CIF_DD9 | Camera data signal |
| 86 | CIF_FV | Camera frame clock |
| 88 | CIF_MCLK | Camera master clock |
| 90 | CIF_PIXCLK | Camera pixel clock |
| 92 | CIF_LV | Camera line clock |
| 127 | not connected | |
| 129 | USBHPEN1 | Power control to USB ports |
| 131 | USBHPWR1 | USB over-current indicator |
| 133 | not connected | |

A.4 Hilscher COM-Module connector

TABLE 11.

J1 - Hilscher COM-Module connector

| Pin | Signal Trizeps III PXA255 | Signal Trizeps IV PXA270 | Description | Direction |
|-----|-------------------------------------|-------------------------------------|---|-----------|
| 1 | GND | GND | Ground | - |
| 2 | +3V3 | +3V3 | Power Supply | - |
| 3 | OUTPUT1/BD01 | OUTPUT1/BD01 | TTL Output 01 / buffered data line 01 | out / bi |
| 4 | OUTPUT0/BD00 | OUTPUT0/BD00 | TTL Output 00 / buffered data line 00 | out / bi |
| 5 | OUTPUT3/BD03 | OUTPUT3/BD03 | TTL Output 03 / buffered data line 03 | out / bi |
| 6 | OUTPUT2/BD02 | OUTPUT2/BD02 | TTL Output 02 / buffered data line 02 | out / bi |
| 7 | OUTPUT5/BD05 | OUTPUT5/BD05 | TTL Output 05 / buffered data line 05 | out / bi |
| 8 | OUTPUT4/BD04 | OUTPUT4/BD04 | TTL Output 04 / buffered data line 04 | out / bi |
| 9 | OUTPUT7/BD07 | OUTPUT7/BD07 | TTL Output 07 / buffered data line 07 | out / bi |
| 10 | OUTPUT6/BD06 | OUTPUT6/BD06 | TTL Output 06 / buffered data line 06 | out / bi |
| 11 | BA02/A2D1 | BA02/A2D1 | buffered address line 02 / multiplexed line | out / bi |
| 12 | BA01/A1D0 | BA01/A1D0 | buffered address line 01 / multiplexed line | out / bi |
| 13 | BA04/A4D3 | BA04/A4D3 | buffered address line 04 / multiplexed line | out / bi |
| 14 | BA03/A3D2 | BA03/A3D2 | buffered address line 03 / multiplexed line | out / bi |
| 15 | BA06/A6D5 | BA06/A6D5 | buffered address line 06 / multiplexed line | out / bi |
| 16 | BA05/A5D4 | BA05/A5D4 | buffered address line 05 / multiplexed line | out / bi |
| 17 | BA08/A8D7 | BA08/A8D7 | buffered address line 08 / multiplexed line | out / bi |
| 18 | BA07/A7D6 | BA07/A7D6 | buffered address line 07 / multiplexed line | out / bi |
| 19 | BA10 | BA10 | buffered address line 10 | out |
| 20 | BA09 | BA09 | buffered address line 09 | out |
| 21 | BA12 | BA12 | buffered address line 12 | out |
| 22 | BA11 | BA11 | buffered address line 11 | out |
| 23 | BA14 | BA14 | buffered address line 14 | out |
| 24 | BA13 | BA13 | buffered address line 13 | out |
| 25 | $\overline{\text{BWE}}$ | $\overline{\text{BWE}}$ | buffered write enable | out |
| 26 | $\overline{\text{CS_HIL}}$ | $\overline{\text{CS_HIL}}$ | chip select Hilscher | out |
| 27 | $\overline{\text{GPIO20/IRQ_HIL}}$ | $\overline{\text{GPIO85/IRQ_HIL}}$ | interrupt request Hilscher | in |
| 28 | $\overline{\text{BOE}}$ | $\overline{\text{BOE}}$ | buffered output enable | out |
| 29 | $\overline{\text{RST_OUT_BUF}}$ | $\overline{\text{RST_OUT_BUF}}$ | buffered RESET_OUT | out |
| 30 | $\overline{\text{BUSY}}$ | $\overline{\text{BUSY}}$ | busy signal Hilscher | out |
| 31 | DIAG_RX0 | DIAG_RX0 | diagnostic receive Hilscher | in |
| 32 | DIAG_TX0 | DIAG_TX0 | diagnostic transmit Hilscher | out |
| 33 | - | | reserved | - |
| 34 | - | | reserved | - |
| 35 | - | | reserved | - |
| 36 | - | | reserved | - |
| 37 | - | | reserved | - |

TABLE 11. J1 - Hilscher COM-Module connector

| Pin | Signal Trizeps III PXA255 | Signal Trizeps IV PXA270 | Description | Direction |
|-----|------------------------------|-----------------------------|-----------------------|-----------|
| 38 | - | | reserved | - |
| 39 | GND | GND | Ground | - |
| 40 | +3V3 | +3V3 | Power Supply | - |
| 41 | - | | reserved | - |
| 42 | - | | reserved | - |
| 43 | - | | reserved | - |
| 44 | - | | reserved | - |
| 45 | - | | reserved | - |
| 46 | - | | reserved | - |
| 47 | - | | reserved | - |
| 48 | - | | reserved | - |
| 49 | - | | reserved | - |
| 50 | (GND) | (GND) | usually not connected | - |

A.5 Extension bus connector

TABLE 12.

J2 - Extension bus connector

| Pin | Signal Trizeps III PXA255 | Signal Trizeps IV PXA270 | Description | Direction |
|-----|------------------------------|-----------------------------|---|-----------|
| 1 | BD08 | BD08 | buffered data line 08 | bi |
| 2 | INPUT07 | INPUT07 | TTL Input 07 | in |
| 3 | BD09 | BD09 | buffered data line 09 | bi |
| 4 | INPUT06 | INPUT06 | TTL Input 06 | in |
| 5 | BD10 | BD10 | buffered data line 10 | bi |
| 6 | INPUT05 | INPUT05 | TTL Input 05 | in |
| 7 | BD11 | BD11 | buffered data line 11 | bi |
| 8 | INPUT04 | INPUT04 | TTL Input 04 | in |
| 9 | BD12 | BD12 | buffered data line 12 | bi |
| 10 | INPUT03 | INPUT03 | TTL Input 03 | in |
| 11 | BD13 | BD13 | buffered data line 13 | bi |
| 12 | INPUT02 | INPUT02 | TTL Input 02 | in |
| 13 | BD14 | BD14 | buffered data line 14 | bi |
| 14 | INPUT01 | INPUT01 | TTL Input 01 | in |
| 15 | BD15 | BD15 | buffered data line 15 | bi |
| 16 | INPUT00 | INPUT00 | TTL Input 00 | in |
| 17 | +3V3 | +3V3 | Power Supply | - |
| 18 | +3V3 | +3V3 | Power Supply | - |
| 19 | GND | GND | Ground | - |
| 20 | GND | GND | Ground | - |
| 21 | AD1 | AD1 | Analog / Digital Input 1 (UCB1400) | in |
| 22 | EXT_CLK | EXT_CLK | External Clock for CPLD | in |
| 23 | AD3 | AD3 | Analog / Digital Input 3 (UCB1400) | in |
| 24 | GP07 | | General purpose IO 07 | bi |
| | | GPIO27_CIF_DD0 | Camera Interface Data 0 | in |
| 25 | GP23 | | General purpose IO 23 | bi |
| | | GPIO106_CIF_DD9 | Camera Interface Data 09 | in |
| 26 | GP09 | | General purpose IO 09 | bi |
| | | GPIO114_CIF_DD1 | Camera Interface Data 01 | in |
| 27 | GP21_TTLIO_IRQ | | General purpose IO 21 | bi |
| | | GPIO108_CIF_DD7 | Camera Interface Data 07 | in |
| 28 | GP11 | | General purpose IO 11 | bi |
| | | GPIO116_CIF_DD2 | Camera Interface Data 02 | in |
| 29 | NSSPTXD | | Network Synchronous Serial port transmit | out |
| | | GPIO25_CIF_LV | Camera Interface Line Clock | in |

TABLE 12. J2 - Extension bus connector

| Pin | Signal Trizeps III PXA255 | Signal Trizeps IV PXA270 | Description | Direction |
|-----|------------------------------|-----------------------------|--|-----------|
| 30 | GP13 | | General purpose IO 13 | bi |
| | | GPIO115_CIF_DD3 | Camera Interface Data 03 | in |
| 31 | NSSPRXD | | Network Synchronous Serial port receive | in |
| | | GPIO26_CIF_PCLK | Camera Interface Pixelclock | in |
| 32 | GP14 | | General purpose IO 14 | bi |
| | | GPIO95_CIF_DD4 | Camera Interface Data 04 | in |
| 33 | NSSPCLK | | Network Synchronous Serial port clock | in |
| | | GPIO23_CIF_MCLK | Camera Interface Masterclock | out |
| 34 | GP16 | | General purpose IO 16 | bi |
| | | GPIO91_CIF_DD5/UCLK | Camera Interface Data 05 | in |
| 35 | NSSPFRM | | Network Synchronous Serial port frame | in |
| | | GPIO24_CIF_FV | Camera Interface frame clock | in |
| 36 | GP17 | | General purpose IO 17 | bi |
| | | GPIO17_CIF_DD6 | Camera Interface Data 06 | in |
| 37 | $\overline{CS4}$ | $\overline{CS4}$ | chip select 4 | out |
| 38 | GP32 | | General purpose IO 32 | bi |
| | | GPIO107_CIF_DD8 | Camera Interface Data 08 | in |
| 39 | I2C Data | GPIO118_I2C Data | I2C Data signal | bi |
| 40 | GPIO00_IRQ_PIC | GPIO00_IRQ_PIC | General purpose IO 0 | bi |
| 41 | I2C_CLK | GPIO117_I2C_CLK | I2C Clock signal | out |
| 42 | - | | reserved for future use | - |
| 43 | GND | GND | Ground | - |
| 44 | GND | GND | Ground | - |
| 45 | +5V | +5V | Power Supply | - |
| 46 | +5V | +5V | Power Supply | - |
| 47 | GND | GND | Ground | - |
| 48 | GND | GND | Ground | - |
| 49 | VIN_FUSED | VIN_FUSED | Power Supply | - |
| 50 | VIN_FUSED | VIN_FUSED | Power Supply | - |

A.6 UPS connector

An UPS is available for the ConXS. The UPS is connected with ConXS via the following connector.

TABLE 13.

J3 - UPS connector

| Pin | Signal | Description |
|-----|-------------------|--|
| 1 | I2C_DATA | data I ² C Bus (PXA255/PXA270) |
| 2 | I2C_CLK / ANGBOOT | clock I ² C Bus (PXA255/PXA270) |
| 3 | +3V3 | Power Supply |
| 4 | BATT_EMPTY | CPLD signal |
| 5 | BATT_EN | CPLD signal |
| 6 | CHARGE | CPLD signal |
| 7 | VIN_FUSED | Power Supply |
| 8 | VIN_FUSED | Power Supply |
| 9 | GND | Ground |
| 10 | GND | Ground |

A.7 JTAG connector (CPLD)

A CPLD is placed on the ConxS which can be programmed through an 6-pin header with the following pinout.

TABLE 14.

J4 - JTAG connector (CPLD)

| Pin | Signal | Description |
|-----|--------|---------------|
| 1 | +3V3 | Power Supply |
| 2 | GND | Ground |
| 3 | XC_TCK | Clock signal |
| 4 | XC_TDO | Output signal |
| 5 | XC_TDI | Input signal |
| 6 | XC_TMS | Mode signal |

A.8 RS232 connector (port 3)

The connector J5 is a male DB9 connector with the following pin description.

TABLE 15.

J5 - Serial Interface connector (port 3)

| Pin | Signal | Description |
|-----|-------------|---------------------|
| 1 | FF_DCD_V24X | Data Carrier Detect |
| 2 | FF_RXD_V24X | Receive Data |
| 3 | FF_TXD_V24X | Transmit Data |

TABLE 15.

J5 - Serial Interface connector (port 3)

| Pin | Signal | Description |
|-----|-------------|---------------------|
| 4 | FF_DTR_V24X | Data Terminal Ready |
| 5 | GND | Ground |
| 6 | FF_DSR_V24X | Data Set Ready |
| 7 | FF_RTS_V24X | Request to Send |
| 8 | FF_CTS_V24X | Clear to Send |
| 9 | FF_RI_V24X | Ring Indicator |

A.9 Power Supply (I)

The Power Supply connector is produced by PHOENIX. It's a 2 pin connector with the part number MSTBVA 2,5/2-G-5,08.

TABLE 16.

J7 - Power Supply

| Pin | Signal | Description |
|-----|--------|--------------|
| 1 | VIN | Power Supply |
| 2 | GND | Ground |

A.10 Ethernet connector

The Ethernet connector is an usually RJ45 connector with integrated traffic LEDs with the following pin description.

TABLE 17.

J8 - Ethernet connector

| Pin | Signal | Description |
|-----|---------------|------------------------------|
| 1 | TD+ | Transmit differential output |
| 2 | TD- | Transmit differential output |
| 3 | RD+ | Receive differential output |
| 4 | CT_T | Center point transmit |
| 5 | CT_R | Center point receive |
| 6 | RD- | Receive differential output |
| 7 | nc | not connected |
| 8 | CHGND | Chassis ground |
| 9 | +3V3 | pullup 1K |
| 10 | ETH_SPEED_100 | Status: Ethernet speed |
| 11 | +3V3 | pullup 1K |
| 12 | ETH_LINK_AKT | Status: Ethernet link |

A.11 USB-A connector

TABLE 18.

J12 - USB-A connector

| Pin | Signal | Description |
|-----|---------|---------------------|
| 1 | VCCB+ | Power Supply |
| 2 | OTG_DM2 | Differential signal |
| 3 | OTG_DP2 | Differential signal |
| 4 | GNDB | Ground |
| 5 | VCCT+ | Power Supply |
| 6 | OTG_DM1 | Differential signal |
| 7 | OTG_DP1 | Differential signal |
| 8 | GNDT | Ground |
| 9 | CHGND | Chassis Ground |
| 10 | CHGND | Chassis Ground |
| 11 | CHGND | Chassis Ground |
| 12 | CHGND | Chassis Ground |

A.12 Display connector

This is an universal LCD connector to connect displays from sub 1/4 VGA to 16bpp TFT SVGA, LVDS or DVI extensions available. table 19 on page 38 describes the pins and their functions.

TABLE 19.

J14 - Display connector (40-pin Header)

| Pin | Signal | Description |
|-----|--------|---|
| 1 | LDD00 | LCD controller display data (PXA255/PXA270) |
| 2 | LDD01 | LCD controller display data (PXA255/PXA270) |
| 3 | LDD02 | LCD controller display data (PXA255/PXA270) |
| 4 | LDD03 | LCD controller display data (PXA255/PXA270) |
| 5 | LDD04 | LCD controller display data (PXA255/PXA270) |
| 6 | LDD05 | LCD controller display data (PXA255/PXA270) |
| 7 | LDD06 | LCD controller display data (PXA255/PXA270) |
| 8 | LDD07 | LCD controller display data (PXA255/PXA270) |
| 9 | LDD08 | LCD controller display data (PXA255/PXA270) |
| 10 | LDD09 | LCD controller display data (PXA255/PXA270) |
| 11 | LDD10 | LCD controller display data (PXA255/PXA270) |
| 12 | LDD11 | LCD controller display data (PXA255/PXA270) |
| 13 | LDD12 | LCD controller display data (PXA255/PXA270) |
| 14 | LDD13 | LCD controller display data (PXA255/PXA270) |

TABLE 19.

J14 - Display connector (40-pin Header)

| Pin | Signal | Description |
|-----|----------------|--|
| 15 | LDD14 | LCD controller display data (PXA255/PXA270) |
| 16 | LDD15 | LCD controller display data (PXA255/PXA270) |
| 17 | L_FCLK | LCD frame clock (PXA255/PXA270) |
| 18 | L_LCLK | LCD line clock (PXA255/PXA270) |
| 19 | L_PCLK | LCD pixel clock (PXA255/PXA270) |
| 20 | L_BIAS | LCD ac bias drive (PXA255/PXA270) |
| 21 | TSMX | negative X-plate touch screen (Trizeps - UCB 1400) |
| 22 | TSMY | negative Y-plate touch screen (Trizeps - UCB 1400) |
| 23 | TSPX | positive X-plate touch screen (Trizeps - UCB 1400) |
| 24 | TSPY | positive Y-plate touch screen (Trizeps - UCB 1400) |
| 25 | L_DISP | LCD on |
| 26 | NC | not connected |
| 27 | +3V3 | Power supply |
| 28 | GND | Ground |
| 29 | +5V | Power supply |
| 30 | GND | Ground |
| 31 | VIN_FUSED | Power supply |
| 32 | GND | Ground |
| 33 | GND | Ground |
| 34 | GND | Ground |
| 35 | I2C_DATA | Data I ² C Bus (PXA255/PXA270) |
| 36 | I2C_CLK | Clock I ² C Bus (PXA255/PXA270) |
| 37 | GPIO00_IRQ_PIC | Interrupt of the PIC (optional) |
| 38 | V_CONTRAST | Contrast voltage |
| 39 | NC | not connected |
| 40 | BL_POWER | Backlight power |

A.13 Serial port 1 connector

Signals of serial port 1 are available at this 10-pin header.

TABLE 20.

J18 - Serial port 1 connector

| Pin | Signal | Description |
|-----|--------------|-------------------------------------|
| 1 | - | internally connected to Pin 2 and 7 |
| 2 | - | internally connected to Pin 1 and 7 |
| 3 | COM2_TXD_V24 | Transmit Data |
| 4 | COM2_CTS_V24 | Clear To Send |
| 5 | COM2_RXD_V24 | Receive Data |

TABLE 20.

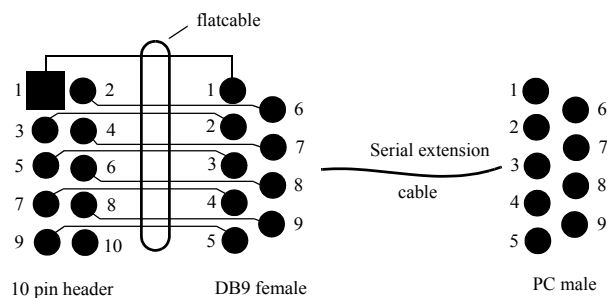
J18 - Serial port 1 connector

| Pin | Signal | Description |
|-----|--------------|-------------------------------------|
| 6 | COM2_RTS_V24 | Request To Send |
| 7 | - | internally connected to Pin 1 and 2 |
| 8 | (+3V3) | (Power Supply) |
| 9 | GND | Ground |
| 10 | nc | not connected |

If you want to connect J18 with a PC you can use the solution shown in figure 7 on page 40:

FIGURE 7.

Connection of the serial interface header (J18) to the PC



A.14 USB / IrDA connector

USB and IrDA signals are available at connector J20.

TABLE 21.

J20 - USB and IrDA Connector

| Pin | Signal | Description |
|-----|-----------|------------------------------|
| 1 | GND | Ground |
| 2 | +3V3 | Power Supply |
| 3 | DIAG_RX0 | diagnostic receive Hilscher |
| 4 | DIAG_TX0 | diagnostic transmit Hilscher |
| 5 | +3V3 | Power Supply |
| 6 | TXD_2 | Transmit data |
| 7 | RXD_2 | Receive data |
| 8 | IRDA_MODE | |
| 9 | IRDA_SD | |
| 10 | GND | Ground |

A.15 OTG connector

TABLE 22.

J21 - OTG connector

| Pin | Signal | Description |
|-----|---------|---------------------|
| 1 | VCC+ | Power Supply |
| 2 | OTG_DM2 | differential signal |
| 3 | OTG_DP2 | differential signal |
| 4 | OTG_ID | |
| 5 | GND | Ground |

A.16 USB-B connector

TABLE 23.

J22 - USB-B connector

| Pin | Signal | Description |
|-----|--------|---------------------|
| 1 | VCC+ | Power Supply |
| 2 | TUDC- | differential signal |
| 3 | TUDC+ | differential signal |
| 4 | GND | Ground |

A.17 MultiMediaCard connector

The MultiMediaCard connector has the following pinout:

| Pin | Signal PXA255 (Trizeps III) | Description | Signal PXA270 (Trizeps IV) | Description |
|-----|--------------------------------|------------------------------------|-------------------------------|------------------------------------|
| 1 | GPIO08_MMC_CS0 | MMC chip select | MMCDAT3 | MMC data 3 |
| 2 | MMC_CMD | MMC command | MMCCMD | MMC command |
| 3 | GND | Ground | GND | Ground |
| 4 | +3V3 | Power supply | +3V3 | Power supply |
| 5 | GPIO06_MMC_CLK | MMC clock | MMCCLK | MMC clock |
| 6 | GND | Ground | GND | Ground |
| 7 | MMC_DAT | MMC data | MMCDAT0 | MMC data 0 |
| 8 | nc | not connected | MMCDAT1 | MMC data 1 |
| 9 | nc | not connected | MMCDAT2 | MMC data 2 |
| 10 | GPIO12_MMC_DET | MMC card detect (100K pulldown) | MMCDET | MMC card detect (100K pulldown) |
| 11 | +3V3 | Power supply | +3V3 | Power supply |
| 12 | GND | 100k pulldown | GND | 100k pulldown |
| 13 | nc | not connected | nc | not connected |

A.18 Speaker connector

Connect a speaker to JJ3.

TABLE 24.

JJ3 - Speaker connector

| Pin | Signal | Description |
|-----|---------------|-------------------------|
| 1 | HEADPHONE_R | Speaker positive signal |
| 2 | HEADPHONE_GND | Speaker negative signal |

A.19 Microphone connector

Connect a microphone to JJ2.

TABLE 25.

JJ2 - Microphone connector

| Pin | Signal | Description |
|-----|---------|--------------------------|
| 1 | MIC_OUT | Microphone output signal |
| 2 | MIC_GND | Microphone ground |

A.20 Backlight power select connector

By setting this jumper you can decide to supply your backlight inverter with +5V or VIN-FUSED.

TABLE 26.

JJ4 - Backlight power select connector

| Pin | Signal | Description |
|-----|-----------|-----------------|
| 1 | VIN_FUSED | Input voltage |
| 2 | BL_POWER | Backlight power |
| 3 | +5V | +5V supply |

A.21 Reset connector

For normal operation this jumper is left open. For resetting the board connect $\overline{\text{RESIN}}$ to GND.

TABLE 27.

JJ5 - Reset connector

| Pin | Signal | Description |
|-----|---------------------------|-------------|
| 1 | GND | Ground |
| 2 | $\overline{\text{RESIN}}$ | Reset in |

A.22 Code select connector

This is an jumper to set the CPLD

TABLE 28.

JJ6 - Code select connector

| Pin | Signal | Description |
|-----|------------|----------------|
| 1 | CPLD_INPUT | 100K pulled up |
| 2 | GND | Ground |

A.23 Angelboot

You can start the firmware by closing JJ8 when powering up.

TABLE 29.

JJ8 - Angel boot connector

| Pin | Signal | Description |
|-----|-----------|-------------|
| 1 | ANGELBOOT | Angel boot |
| 2 | GND | Ground |

A.24 Audio stereo connector

The audio stereo connector has the following pinout:

TABLE 30.

U1 - Audio stereo connector

| Pin | Signal | Description |
|-----|---------------|------------------|
| 1 | HEADPHONE_GND | Headphone Ground |
| 2 | HEADPHONE_L | Headphone left |
| 3 | HEADPHONE_R | Headphone right |

A.25 CompactFlash connector

TABLE 31.

U7 - CompactFlash Connector

| Pin | Signal | Description |
|-----|-----------------------|----------------------|
| 1 | GND | Ground |
| 2 | S0_D03 | Databus |
| 3 | S0_D04 | Databus |
| 4 | S0_D05 | Databus |
| 5 | S0_D06 | Databus |
| 6 | S0_D07 | Databus |
| 7 | $\overline{S0_CE1}$ | Card Enable signal |
| 8 | S0_A10 | Memory address bus |
| 9 | S0_OE | Output Enable signal |
| 10 | S0_A09 | Memory address bus |
| 11 | S0_A08 | Memory address bus |
| 12 | S0_A07 | Memory address bus |
| 13 | S0_VDD | Power Supply |
| 14 | S0_A06 | Memory address bus |
| 15 | S0_A05 | Memory address bus |
| 16 | S0_A04 | Memory address bus |
| 17 | S0_A03 | Memory address bus |
| 18 | S0_A02 | Memory address bus |
| 19 | S0_A01 | Memory address bus |
| 20 | S0_A00 | Memory address bus |
| 21 | S0_D00 | Databus |
| 22 | S0_D01 | Databus |
| 23 | S0_D02 | Databus |
| 24 | $\overline{S0_IOIS}$ | Write Protect signal |
| 25 | $\overline{S0_CD2}$ | Card Detect signal |
| 26 | $\overline{S0_CD1}$ | Card Detect signal |
| 27 | S0_D11 | Databus |
| 28 | S0_D12 | Databus |
| 29 | S0_D13 | Databus |
| 30 | S0_D14 | Databus |
| 31 | S0_D15 | Databus |
| 32 | $\overline{S0_CE2}$ | Card Enable signal |
| 33 | $\overline{S0_VSI}$ | Voltage Sense signal |
| 34 | $\overline{S0_IOR}$ | I/O Read signal |
| 35 | $\overline{S0_IOW}$ | I/O Write signal |
| 36 | $\overline{S0_WE}$ | Write Enable signal |
| 37 | $\overline{S0_RDY}$ | Ready / Busy signal |

TABLE 31.

U7 - CompactFlash Connector

| Pin | Signal | Description |
|-----|-----------------------|--|
| 38 | S0_VDD | Power Supply |
| 39 | nc | not connected |
| 40 | $\overline{S0_VS2}$ | Voltage Sense signal |
| 41 | S0_RESET | Reset signal |
| 42 | $\overline{S0_WAIT}$ | Wait signal |
| 43 | nc | not connected |
| 44 | $\overline{S0_REG}$ | Attribute-Memory-Select or Register signal |
| 45 | S0_BVD2 | Battery Voltage Detect signal |
| 46 | S0_BVD1 | Battery Voltage Detect signal |
| 47 | S0_D08 | Databus |
| 48 | S0_D09 | Databus |
| 49 | S0_D10 | Databus |
| 50 | GND | Ground |

A.26 Microphone connector

The microphone connector has the following pinout:

TABLE 32.

U14 - Microphone connector

| Pin | Signal | Description |
|-----|---------|-------------------|
| 1 | MIC_GND | Microphone Ground |
| 2 | nc | not connected |
| 3 | MIC_OUT | Microphone out |

A.27 On board peripherals (address code)

TABLE 33.

On board peripherals

| Offset ($\overline{CS3}$) | Device | Address Trizeps III |
|-----------------------------|--|------------------------|
| 0x00000000 | READ: PCMCIA Status | 0x0C000000 |
| 0x00800000 | R/W: SMSC91C96 | 0x0C800000 |
| 0x01000000 | R/W: CAN SJA1000 | 0x0D000000 |
| 0x01800000 | WRITE: TTL OUTPUT READ: TTL INPUT | 0x0D800000 |
| 0x02000000 | WRITE: PCMCIA CTL READ: PCMCIA STATUS | 0x0E000000 |
| 0x02400000 | WRITE: IrDA | 0x0E400000 |
| 0x02800000 | R/W: UPS | 0x0E800000 |
| 0x03000000 | RESERVED | 0x0F000000 |
| 0x03800000 | WRITE: EEPOT (display contrast) | 0x0F800000 |

Revision

Board: ConXS

TABLE 34.

| Revision | PCB number | Date | Changes |
|----------|------------|------------|--|
| 1.0 | 01_01_04 | 28.03.2004 | ----- |
| 1.1 | 01_01_04 | 02.09.2004 | The signal name of Pin 73 of SODIMM200 is changed to GPIO32 |
| 1.2 | 03_06_05 | 17.08.05 | GPIO table for PXA270 added, GPIOs overworked, Battery Connector removed, BT progr. Connector removed |
| 1.3 | 03_06_05 | 07.11.05 | MMC corrected, Extension Bus PXA270 Signals added |
| 1.31 | 03_06_05 | 20.12.05 | signal description for GP[105] added |
| 1.32 | 03_06_05 | 10.02.06 | SODIMM pin numbers added (Table 3/4) |
| 1.33 | 03_06_05 | 28.07.06 | JJ2 and JJ3 interchanged |
| 1.34 | 03_06_05 | 23.02.07 | 3.13 Page 17 TTLIO Portadr fixed |
| 1.35 | 03_06_05 | 28.04.09 | Page 35 Table 12 Col 2: Pin 38 is GPIO32 (not GPIO22) Page 35 Table 12 Col 3: Pin 34 is GPIO91 (not GPIO94) |
| | | | |

FIGURE 8. Dimensions of ConXS board (top side)

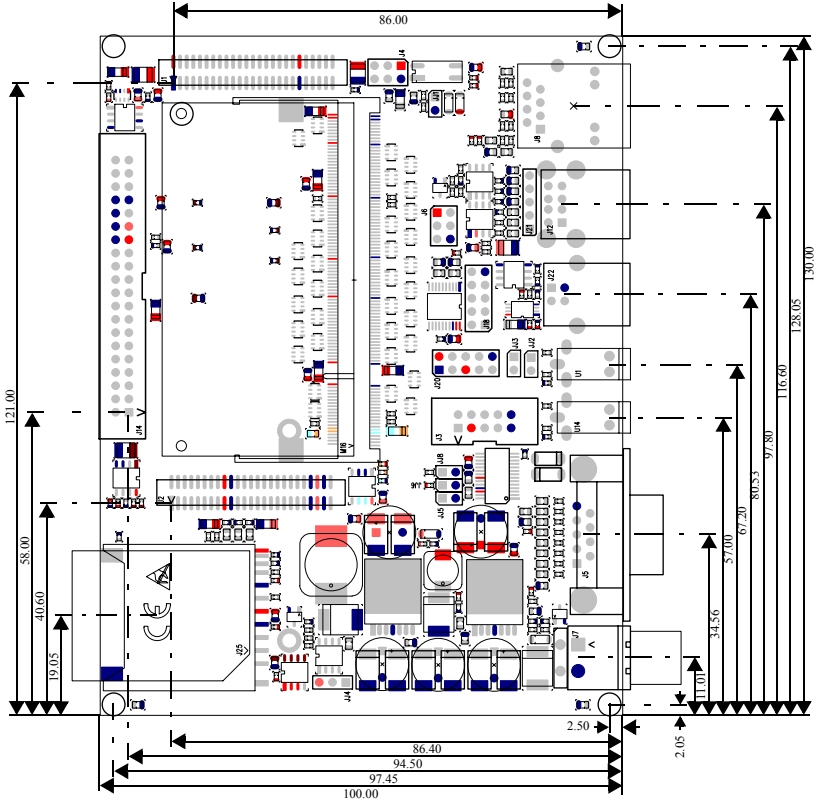


FIGURE 9. Dimension of ConXS board (bottom side)

