

Trizeps-II-270M Module (Rev. 0.1)



1.0 Introduction

The Trizeps-II-270M Module is based on the Intel/Marvell® XScale™ Core CPU 88AP270M (312, 416, 520 and 624 MHz) ARM® Architecture v.5TE compliant and application code compatible with Intel® SA-1110 and PXA2xx processor which are used on the Trizeps I, Trizeps II, Trizeps III and Trizeps IV Modules. The CPU is based on Intel/Marvell® Superpipelined RISC technology for high core speeds at low power (860K Dhrystone 2.1 per second @ 520 MHz). It includes Intel/Marvell® Wireless MMX® technology, enabling high performance, low-power multimedia acceleration with a general-purpose instruction set. Intel/Marvell® Quick Capture technology provides one of the industry's most flexible and powerful camera interfaces for capturing digital images and video. While performance is key, power consumption is also a critical component. The new capabilities of Wireless Intel SpeedStep® technology provide a quantum leap forward in low-power operation.

Some features of the 88AP270M: Integrated memory and PCMCIA/CompactFlash Controller with 100MHz Memory Bus. System Control Module includes general-purpose interruptible I/O ports, real-time clock, watchdog and interval timers, power management controller, interrupt and reset controller, LCD controller and two on-chip oscillators. Trizeps-II-270M includes also the Philips UCB 1400, on a single chip it combines audio codec functions, a touch-screen controller and power management interfaces. The incorporated A/D converter and the touch screen interface provides complete control and read-out of a 4 wire resistive touch screen.

Features of Trizeps-II-270M:

Marvell XScale 88AP270M 312...624 MHz

16 or 32 Bit Intel P33 Flash 16..64MB

uSD-Card-Slot

Reset Generator

Pin compatible to Trizeps I / II

UCB 1400 codec with audio and touch

32 Bit LP SDRAM (64..128 MB)

High-Eff. switching core-voltage regulator supporting SpeedStep® Features

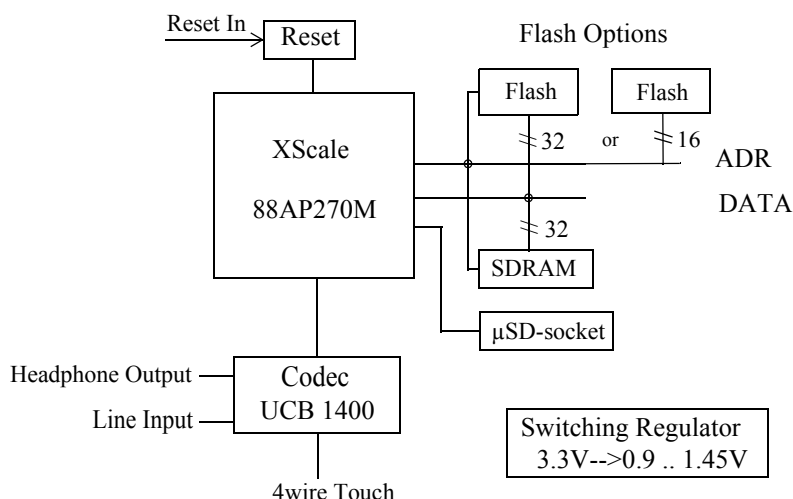
2.0 Functional description of the Trizeps-II-270M Module

In the following you'll find special information about the Trizeps-II-270M Module. For more information concerning the 88AP270M and the UCB1400 please refer to Marvell's XScale manual and Philips data sheet of the UCB 1400.

2.1 Components of the Trizeps-II-270M Module

Figure 1.

Trizeps-II-270M Module



Components of the Trizeps-II-270M Module:

1. Marvell XScale 88AP270M (microprocessor)
2. UCB 1400 (a single chip, stereo audio codec equipped with touch screen and power management interfaces), IRQ GP01
3. SDRAM 32-Bit wide @ bank 0
4. Flash: Intel Strata® Flash (P33) 16- or 32-Bit wide @ nCS0 or / and nCS1
5. Switching-mode core voltage regulator with I²C management interface
6. μSD-Socket (also wired to SODIMM)
7. Reset generator

2.2 Interfaces of the XScale 88AP270M on SODIMM socket

The Trizeps-II-270M Module offers the following interfaces:

2.2.1 Universal Asynchronous Receiver / Transmitter (UART) serial ports

The XScale 88AP270M processor has three UARTs: Full Function UART (FFUART), Bluetooth UART (BLUART), and Standard UART (STUART).

The UARTs share the following features:

- Functionally compatible with the 16550
- Ability to add or delete standard asynchronous communications bits (start, stop and parity) in the serial data
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud rate generator that allows the internal clock to be divided by 1 to $(2^{16}-1)$ to generate an internal 16X clock
- Modem control pins that allow flow control through software

Full Function UART: All of the modem signals are accessible on the SODIMM socket.

Bluetooth UART: The signals TxD, RxD, CTS and RTS are accessible on the SODIMM socket.

Standard UART: The signals IRRxD and IRTxD are accessible on the SODIMM socket. This serial port can work as Fast Infrared Communications Port (FICP). It operates at half-duplex and provides direct connection to commercially available Infrared Data Association (IrDA) compliant LED transceivers. The FICP is based on the 4-Mbps IrDA standard and uses four-position pulse modulation (4PPM) and a specialized serial packet protocol developed for IrDA transmission. To support the standard, the FICP has:

- A bit Encoder / Decoder
- A serial-to-parallel data engine
- A transmit FIFO 128 entries deep and 8 bits wide
- A receive FIFO 128 entries deep and 11 bits wide

The FICP shares GPIO pins for transmit and receive data with the Standard UART. Only one of the ports can be used at a time.

2.2.2 Universal Serial Bus (USB) Device Controller (UDC)

The UDC supports 16 endpoints and can operate half-duplex at a rate of 12Mbps (as a slave only, not as a host or hub controller). The UDC supports four device configurations. Configuration 1, 2 and 3 each supports two interfaces. This allows the host to accommodate dynamic changes in the physical bus topology. A configuration is a specific combination of USB resources available on the device. An interface is a related set of endpoints that present a device feature or function to the host.

2.2.3 Universal Serial Bus (USB) Host Controller

The 88AP270M has one dedicated USB Host Port and another Port which can be driven as Host or as a combined OTG Port, which supports the dynamic role change between Upstream/Downstream Ports (Host/Function). These ports can be driven with speedgrades FS and LS.

Note: Only 2xUSB-Host or 1xUSB-Host and 1xUSB-Device is supported. WinCE-Software automatically disables USB-Host-Port 2, when an USB-Device-Cable is plugged. Use a hub on USB-Host-Port 1, if additional USB-Host ports are needed.

2.2.4 Synchronous Serial Port Controller

The Synchronous Serial Port Controller (SSPC) is a full-duplex synchronous serial interface and can connect to a variety of external analog-to-digital (A/D) converters,

audio and telecom codec, and other devices that use serial protocols for transferring data. The SSPC supports National's Microwire, Texas Instruments' Synchronous Serial Protocol (SSP), and Motorola's Serial Peripheral Interface (SPI) protocol.

The SSPC operates in master mode (the attached peripheral functions as a slave) and supports serial bit rates from 7.2 KHz to 1.84 MHz. Serial data formats may range from 4 to 16 bits in length. The SSPC provides 16 entries deep x 16 bits wide transmit and receive data FIFOs.

The FIFOs may be loaded or emptied by the Central Processor Unit (CPU) using programmed I/O, or DMA burst transfers of 4 or 8 half-words per transfer while receiving or transmitting.

2.2.5 I²C Bus Interface Unit

The I²C bus was created by the Phillips Corporation and is a serial bus with a two-pin interface. The SDA data pin is used for input and output functions and the SCL clock pin is used to control and reference the I²C bus. The I²C bus unit allows the 88AP270M to serve as a master and slave device that resides on the I²C bus.

The I²C unit enables the 88AP270M to communicate with I²C peripherals and microcontrollers for system management functions. The I²C bus requires a minimum amount of hardware to relay status and reliability information concerning the 88AP270M subsystem to an external device.

The I²C unit is a peripheral device that resides on the 88AP270M internal bus. Data is transmitted to and received from the I²C bus via a buffered interface. Control and status information is relayed through a set of memory-mapped registers. Refer to *The I²C-Bus Specification* for complete details on I²C bus operation.

2.2.6 MultiMediaCard Controller / SD / SDIO - Card Controller

The 88AP270M MultiMediaCard (MMC) controller acts as a link between the software used to access the 88AP270M and the MMC stack (a set of memory cards). The MMC controller is designed to support the MMC system, a low-cost data storage and communications system. The 88AP270M MMC controller is based on the standards outlined in *The MultiMediaCard System Specification Version 2.1* with the exception that one- and three-byte data transfers are not supported and the maximum block length is 1023.

The MMC controller features:

- Data transfer rates up to 20 Mbps
- A response FIFO
- Dual receive data FIFOs
- Dual transmit data FIFOs
- Support for two MMCs in either MMC or SPI mode

The MMC-signals are either available at the SODIMM144 socket or at the μ SD-socket on the module.

2.3 Codec (UCB 1400)

Trizeps-II-270M includes also the Philips UCB 1400. It integrates an AC '97 Rev. 2.1 interface for communication to Marvell® XScale processor. If you need a detailed description please refer to Philips data sheet. For interrupt programming of the codec use GP02 (IRQ). GP02 is a general purpose input/output of the 88AP270M.

Features of the UCB 1400:

- Integrated AC '97 Rev. 2.1 interface.
- 20-bit stereo audio codec with programmable sample rates, input and output gain, digital sound processing, capable of driving headphones, and connecting to microphone and line level inputs.
- 4-wire resistive touch screen interface circuit supporting position, pressure and plate resistance measurements.
- 10-bit successive approximation ADC with internal track-and-hold circuit and analog multiplexer for touch screen readout and monitoring of four external high voltage (7.5 V) sources.
- Ten general purpose input/output pins.
- 3.3 V supply voltage and built-in power saving modes for portable and battery-powered applications.

2.4 Memory

The XScale 88AP270M has three different memory spaces: SDRAM, Static Memory, and Card Memory.

SDRAM has four partitions, Static Memory has six, and Card space has two. When memory access attempts to burst across the boundary between adjacent partitions, ensure that the configurations for the partitions are identical. The configurations must be identical in every aspect, including external bus width and burst length.

2.4.1 SDRAM interface

The 88AP270M supports the SDRAM interface, which supports four 16- and 32-bit-wide SDRAM partitions. Each partition is allocated 64 or 256 MBytes of the internal memory map, but the actual size of each partition depends on the SDRAM configuration.

The Trizeps-II-270M uses the first ($\overline{\text{SDCS}}[0]$) of the four partition selects and 32 data-lines. Usually the memory size of SDRAM is 64 MByte, configuration with 128 MByte is also possible.

2.4.2 Static Memory interface / Variable Latency I/O interface

The static memory and variable latency I/O interface has six chip selects ($\overline{\text{CS}}[5:0]$) and 26 bits of byte address ($A[25:0]$) for access up to 64 MBytes of memory in each of six banks. Each chip select is individually programmed for selecting one of the supported static memory types:

- Non-burst ROM or Flash memory is supported on $\overline{\text{CS}}[5:0]$
- Burst ROM or Flash (with non-burst writes) is supported on $\overline{\text{CS}}[5:0]$
- Burst and non-burst SRAM is supported on $\overline{\text{CS}}[5:0]$
- Variable Latency I/O is supported on $\overline{\text{CS}}[5:0]$
- Synchronous static memory is supported on $\overline{\text{CS}}[3:0]$

The Trizeps-II-270M NOR Flash memory is selected usually by the $\overline{\text{CS}}[0]$ ($\overline{\text{CS}}[1]$ optionally, depending on the given configuration of 16 or 32 data-lines). The size of the Flash memory can vary between 16 and 64 MByte.

2.4.3 16-Bit PC Card / Compact Flash Interface

The 88AP270M card interface is based on *The PC Card Standard - Volume 2 - Electrical Specification, Release 2.1*, and *CF+ and CompactFlash Specification Revision 1.4*. The 16-bit PC Card / Compact Flash interface provides control signals to support any combination of 16-bit PC Card / Compact Flash for two card sockets, using address line (A[25:0]) and data lines (D[15:0]).

The PXA255 16-bit PC Card / Compact Flash Controller provides the following signals:

- $\overline{\text{PREG}}$ is muxed with A[26] and selects register space (I/O or attribute) versus memory space
- $\overline{\text{POE}}$ and $\overline{\text{PWE}}$ allow memory and attributes reads and writes
- $\overline{\text{PIOR}}$, $\overline{\text{PIOW}}$ and $\overline{\text{PIOIS16}}$ control I/O reads and writes
- $\overline{\text{PWAIT}}$ allows extended access times
- $\overline{\text{PCE2}}$ and $\overline{\text{PCE1}}$ are byte select high and low for a 16-bit data bus
- PSKTSEL selects between two card sockets

Keith & Koep GmbH uses a small external logic to switch the power to the card-interface and drive external buffers, which are needed to build a hotplug save system. There is also a buffer to read status signals like the BVDDx and VSx signals. Using the reference schematics, you can be sure to be compatible with Keith&Koep's bootloader and OS adaptations.

2.5 Voltage converter (ISL6271CR)

The Trizeps-II-270M Module uses a single power supply of +3V3. To generate the different voltages needed for the 88AP270M a highly integrated power supply system with a high efficiency switch-mode voltage converter is used. The core voltage can be adjusted dynamically through a dedicated I²C interface.

2.6 Reset generator

Resetting the board is possible by using the $\overline{\text{RESET_IN}}$ input or by using the JTAG Reset Input.

2.7 JTAG / Debug Port

The JTAG / Debug port consists of several shift registers, with the destination controlled by the TMS pin and data I/O with TDI / TDO. The JTAG / Debug port provides two different functionalities:

- Programming Flash memory by pushing data through the shift registers
- Hardware-testing using boundary scan interface according to IEEE 1149.1

3.0 Firmware:

The Trizeps-II-270M firmware package includes:

1. PBL (Primary Bootstrap Loader)
2. BOOTP/ TFTP Bootstrap Loader (Keith & Koep GmbH). It offers the following features:
 1. BOOTP/TFTP download with Ethernet support
 2. Special download with simple serial protocol
 3. Flash support
 4. On board selftest
 5. SD/MMC Support (including FAT)

3.1 Bootstrap procedure

After reset the processor starts the PBL (Primary Boot Loader). The PBL sets up the memory system and the MMU and decides to enter the Boot Loader or a customer program. The communication goes via FF_RXD (P.31), FF_TXD (P.33). You can find more information about booting using the document „bootloader2.pdf“.

4.0 DC operating conditions xxx

- | | |
|---|--------|
| 1. Supply voltage | 3.3 V |
| 2. Typical operating current @ 520MHz, 64MB SDRAM | |
| Running | 384 mA |
| Idle | 163 mA |
| Suspend | 2.5 mA |

4.1 Operating temperature:

standard: 0° ... +70°C

industrial available: -20° ...+85°C

4.2 Storage temperature

-40...+125°C

4.3 Humidity

<= 95% (non-condensing) for operating and storage

5.0 Ordering Information

Product specification	Ordering number
1. Trizeps II-270M/C520/R64/ P33.32.2/COD/RoHS	25003
2. Trizeps II-270M/C312/R64/ P33.32.2/COD/RoHS	25023
3. Trizeps II-270M/C520/R64/ P33.32.1/COD/RoHS	25103
4. Trizeps II-270M/C312/X64/ P33.32.2/COD/RoHS	25243
5. Trizeps II-270M/C520/R128/ P33.64.2/COD/RoHS	25283
6. Trizeps II-270M/C520/R128/ P33.32.2/COD/RoHS	25303
7. Trizeps II-270M/C624/R128/ P33.64.2/COD/RoHS	25323

Explanation: xxx

Trizeps II-270M/temperature range, MHz/SDRAM MB/Flash type and MB/UCB Codec/RoHS

Example Position 3:

Trizeps II-270M/commercial temp. range 520MHz/64MB SDRAM/P33 Flash, 32MB arranged with 1 device/UCB Codec/RoHS

Example Position 7:

Trizeps II-270M/commercial temp. range 624MHz/128MB SDRAM/P33 Flash, 64MB arranged with 2 devices/UCB Codec/RoHS

6.0 Pinout information and description

All of the significant signals are accessible via the 144-pin SODIMM socket.

TABLE 1.

Pinout information of the connector J2 of the Trizeps-II-270M Module (144-pin SODIMM-socket)

Pin	Name	Description
1	TSMY	Touch screen negative Y-plate (UCB 1400)
2	TSMX	Touch screen negative X-plate (UCB 1400)
3	TSPY	Touch screen positive Y-plate (UCB 1400)
4	TSPX	Touch screen positive X-plate (UCB 1400)
5	MIC_OUT	Microphone input signal (UCB 1400)
6	FF_RI / GP38	Full function UART Ring Indicator pin (88AP270M)
7	MIC_GND	Microphone ground switch input (UCB 1400)
8	LINEIN_R	Line in right channel (UCB1400)
9	HEADPHONE_R	Line out right channel (UCB1400)
10	LINEIN_L	Line in left channel (UCB1400)
11	HEADPHONE_GND	Reference voltage for headphone drivers (UCB1400)
12	HEADPHONE_L	Line out left channel (UCB1400)
13	AD3	Analog voltage input (UCB 1400)
14	AD2	Analog voltage input (UCB 1400)
15	AD1	Analog voltage input (UCB 1400)
16	AD0	Analog voltage input (UCB 1400)
17	VSSA	Analog Ground (UCB1400)
18	GND	Ground
19	MMCDAT0 / (LDD16)	Multimedia Card data (88AP270M) LCD display data (88AP270M)
20	MMCCLK	Multimedia Card clock(88AP270M, GP114)
21	MMCCMD	Multimedia Card command(88AP270M, GP27)
22	MMCDAT2 / (LDD17)	Multimedia Card data (88AP270M) LCD display data (88AP270M)
23	$\overline{\text{RESET_IN}}$	Reset input (TLC7733)
24	MMCDET	Multimedia Card detect (88AP270M, GP12)
25	$\overline{\text{RESET_OUT}}$	Reset output (88AP270M)
26	L_BIAS	LCD AC bias drive (88AP270M, GP77)
27	BT_RXD	Bluetooth UART Receive pin (88AP270M, GP42)
28	MMCDAT1 / (BATT_FAULT)	Multimedia Card data (88AP270M) Battery fault - main power is going down (88AP270M)
29	BT_TXD	Bluetooth UART Transmit pin (88AP270M, GP43)
30	RXD_2	Standard UART and ICP (88AP270M, GP46)
31	FF_RXD	Full function UART Receive pin (88AP270M, GP96)
32	TXD_2	Standard UART and ICP (88AP270M, GP47)
33	FF_TXD	Full function UART Transmit pin (88AP270M, GP16)

TABLE 1.

Pinout information of the connector J2 of the Trizeps-II-270M Module (144-pin SODIMM-socket)

Pin	Name	Description
34	USBFN- / (TUDC-)	ISP1301 USBOTG- Serial port zero bidirectional (UDC) (88AP270M)
35	VDDA (+3V3)	Analog power supply (UCB 1400)
36	+3V3	Power supply
37	I2C_DATA	I ² C data (88AP270M)
38	USBFN+ / (TUDC+)	ISP1301 USBOTG+ Serial port zero bidirectional (UDC) (88AP270M)
39	SSP_TXD	Synchronous Serial Port Transmit (88AP270M, GP25)
40	I2C_CLK	I ² C clock (88AP270M)
41	SSPS_CLK	Synchronous Serial Port Clock (88AP270M, GP23)
42	SSPS_FRM / PCD	Synchronous Serial Port Frame (88AP270M, GP24)
43	DREQ0	DMA Request (88AP270M, GP115)
44	SSPS_RXD	Synchronous Serial Port Frame (88AP270M, GP26)
45	FF_DCD	Full function UART Data-Carrier-Detect pin (88AP270M, GP10)
46	DREQ1	DMA Request (88AP270M, GP97)
47	FF_DTR	Full function UART Data-Terminal-Ready pin (88AP270M, GP82)
48	$\overline{CS5}$ / (FF_DSR) / USB_P2_8)	Static chip select (88AP270M) Full function UART Data-Set-Ready pin (88AP270M, GP98)
49	FF_RTS	Full function UART Ready-To-Send pin (88AP270M, GP83)
50	FF_CTS	Full function UART Clear-To-Send pin (88AP270M, GP09)
51	BT_RTS	Bluetooth UART Ready-To-Send pin (88AP270M, GP45)
52	BT_CTS	Bluetooth UART Clear-To-Send pin (88AP270M, GP44)
53	PWM1 / (MMCDAT3)	General purpose I/O (88AP270M, GP17) Multimedia Card data (88AP270M, GP111)
54	IRQ_USB_SL / CHOUT0	General purpose I/O (88AP270M, GP105) General purpose I/O (88AP270M, GP108)
55	LDD14	LCD display data (88AP270M, GP72)
56	LDD15	LCD display data (88AP270M, GP73)
57	LDD12	LCD display data (88AP270M, GP70)
58	LDD13	LCD display data (88AP270M, GP71)
59	LDD10	LCD display data (88AP270M, GP68)
60	LDD11	LCD display data (88AP270M, GP69)
61	LDD8	LCD display data (88AP270M, GP66)

TABLE 1.

Pinout information of the connector J2 of the Trizeps-II-270M Module (144-pin SODIMM-socket)

Pin	Name	Description
62	LDD9	LCD display data (88AP270M, GP67)
63	GP00	General purpose I/O (88AP270M, GP00)
64	GP01	General purpose I/O (88AP270M, GP01)
65	GND	Ground
66	GND	Ground
67	L_FCLK	LCD frame clock (88AP270M, GP74)
68	L_LCLK	LCD line clock (88AP270M, GP75)
69	L_PCLK	LCD pixel clock (88AP270M, GP76)
70	LDD6	LCD display data (88AP270M, GP64)
71	LDD7	LCD display data (88AP270M, GP65)
72	LDD4	LCD display data (88AP270M, GP62)
73	LDD5	LCD display data (88AP270M, GP63)
74	LDD2	LCD display data (88AP270M, GP60)
75	LDD3	LCD display data (88AP270M, GP61)
76	LDD0	LCD display data (88AP270M, GP58)
77	LDD1	LCD display data (88AP270M, GP59)
78	GND	Ground
79	$\overline{\text{PWE}}$	PCMCIA CF write enable (88AP270M, GP49)
80	$\overline{\text{POE}}$	PCMCIA CF output enable (88AP270M, GP48)
81	$\overline{\text{PIOW}}$	PCMCIA CF I/O write (88AP270M, GP51)
82	$\overline{\text{PIOR}}$	PCMCIA CF I/O read (88AP270M, GP50)
83	$\overline{\text{PWAIT}}$	PCMCIA CF wait (88AP270M, GP56)
84	$\overline{\text{PIOIS16}}$	I/O select 16 (88AP270M, GP57)
85	$\overline{\text{PREG}}$	PCMCIA register select (88AP270M, GP55)
86	PSKTSEL	PCMCIA socket select (88AP270M, GP54)
87	$\overline{\text{PCE1}}$	PCMCIA card enable 1 (low-byte lane) (88AP270M, GP52)
88	$\overline{\text{PCE2}}$	PCMCIA card enable 2 (high-byte lane) (88AP270M, GP53)
89	+3V3	Power supply
90	+3V3	Power supply
91	D14	Memory data bus (88AP270M)
92	D15	Memory data bus (88AP270M)
93	D12	Memory data bus (88AP270M)
94	D13	Memory data bus (88AP270M)
95	D10	Memory data bus (88AP270M)
96	D11	Memory data bus (88AP270M)
97	D08	Memory data bus (88AP270M)
98	D09	Memory data bus (88AP270M)

TABLE 1.

Pinout information of the connector J2 of the Trizeps-II-270M Module (144-pin SODIMM-socket)

Pin	Name	Description
99	D06	Memory data bus (88AP270M)
100	D07	Memory data bus (88AP270M)
101	D04	Memory data bus (88AP270M)
102	D05	Memory data bus (88AP270M)
103	D02	Memory data bus (88AP270M)
104	D03	Memory data bus (88AP270M)
105	D00	Memory data bus (88AP270M)
106	D01	Memory data bus (88AP270M)
107	GND	Ground
108	GND	Ground
109	RDY / GP18	Variable Latency I/O Ready pin (88AP270M, GP18)
110	\overline{WE}	Memory write enable (88AP270M)
111	RD/ \overline{WR}	Read/Write for static interface (88AP270M)
112	\overline{OE}	Memory output enable (88AP270M)
113	GND	Ground
114	$\overline{CS5}$	Static chip select (88AP270M, GP33)
115	$\overline{CS4}$	Static chip select (88AP270M, GP80)
116	$\overline{CS3}$	Static chip select (88AP270M, GP79)
117	$\overline{CS2}$	Static chip select (88AP270M, GP78)
118	$\overline{CS1}$	Static chip select (88AP270M, GP15)
119	A25	Memory address bus (88AP270M)
120	A24	Memory address bus (88AP270M)
121	A23	Memory address bus (88AP270M)
122	A22	Memory address bus (88AP270M)
123	A21	Memory address bus (88AP270M)
124	A20	Memory address bus (88AP270M)
125	A19	Memory address bus (88AP270M)
126	A18	Memory address bus (88AP270M)
127	A17	Memory address bus (88AP270M)
128	A16	Memory address bus (88AP270M)
129	A15	Memory address bus (88AP270M)
130	A14	Memory address bus (88AP270M)
131	A13	Memory address bus (88AP270M)
132	A12	Memory address bus (88AP270M)
133	A11	Memory address bus (88AP270M)
134	A10	Memory address bus (88AP270M)
135	A09	Memory address bus (88AP270M)
136	A08	Memory address bus (88AP270M)

TABLE 1.

Pinout information of the connector J2 of the Trizeps-II-270M Module (144-pin SODIMM-socket)

Pin	Name	Description
137	A07	Memory address bus (88AP270M)
138	A06	Memory address bus (88AP270M)
139	A05	Memory address bus (88AP270M)
140	A04	Memory address bus (88AP270M)
141	A03	Memory address bus (88AP270M)
142	A02	Memory address bus (88AP270M)
143	A01	Memory address bus (88AP270M)
144	A00	Memory address bus (88AP270M)

You can get detailed information about the socket in the internet (<http://www.amp.com>). Choose search - part number and enter the number 390113-1

TABLE 2.

Pinout information of the connector J4 of the Trizeps-II-270M Module (JST 08FHJ-SM1-TB, 8-pin contact)

Pin	Name	Description
1	+3V3	Power Supply
2	GND	Ground
3	TMS	JTAG test mode select (88AP270M)
4	$\overline{\text{TRST}}$	JTAG test interface reset (88AP270M)
5	TCK	JTAG test clock (88AP270M)
6	TDO	JTAG test data output (88AP270M)
7	TDI	JTAG test data input (88AP270M)
8	$\overline{\text{RESET}}$	Reset input (88AP270M)

TABLE 3.

Pinout information of the connector J5 of the Trizeps-II-270M Module (JST 08FHJ-SM1-TB, 8-pin contact)

Pin	Name	Description
1	+3V3	Power Supply
2	GND	Ground
3	OTG_ID	Identification detector input and output (ISP1301)
4	USBH_P1 (USBOTG+)	USB Host Positive Line (88AP270M) Single-ended DP receiver output (ISP1301)
5	USBH_N1 (USBOTG-)	USB Host Negative Line (88AP270M) Single-ended DM receiver output (ISP1301)
6	VBUS	VBUS line input and output of the USB IF (ISP1301)
7	USBHPWR1	USB Host Power Indicator (88AP270M)
8	USBHPEN1	USB Host Power Enable (88AP270M)

Appendix

7.0 Dimensions of the Trizeps-II-270M Module

Figure 2. Dimensions of the Trizeps-II-270M Module (top view)1

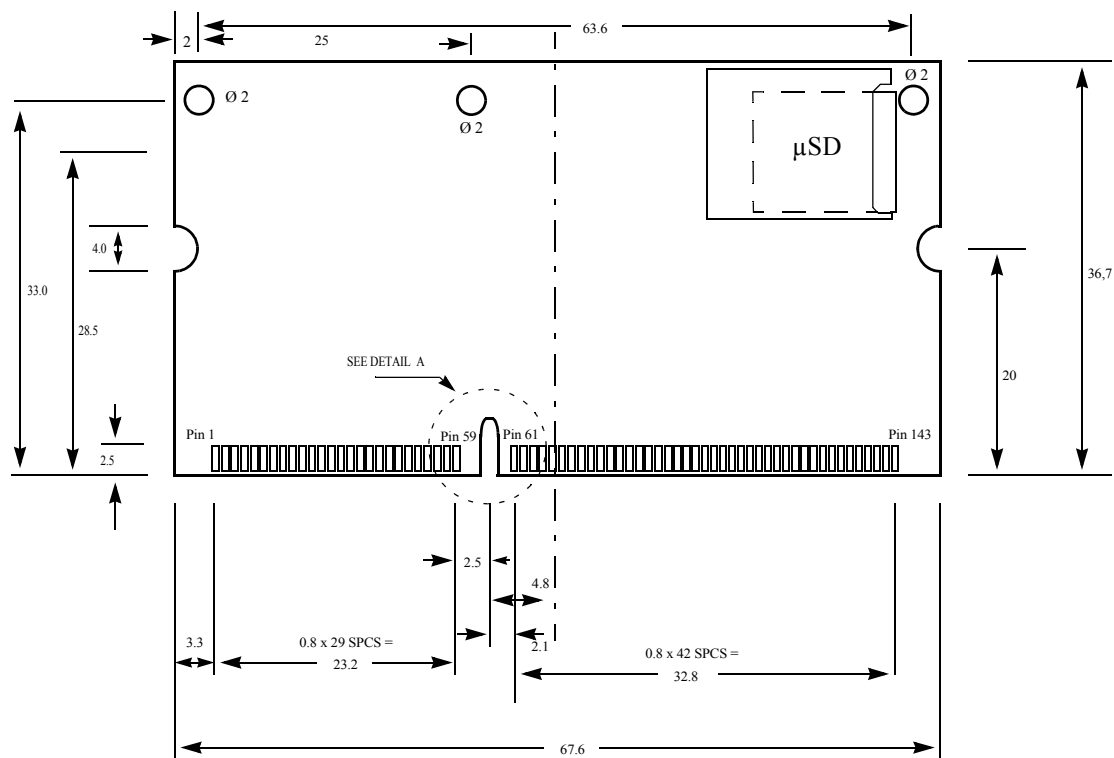


Figure 3. Detail A of Figure 3

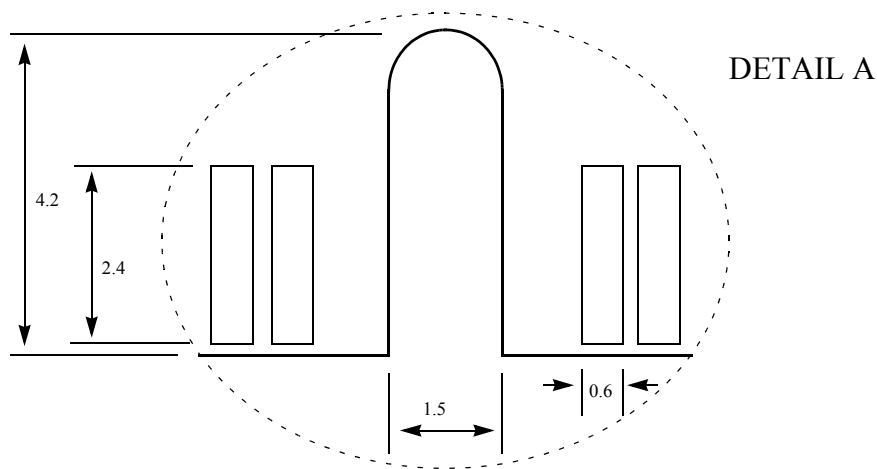
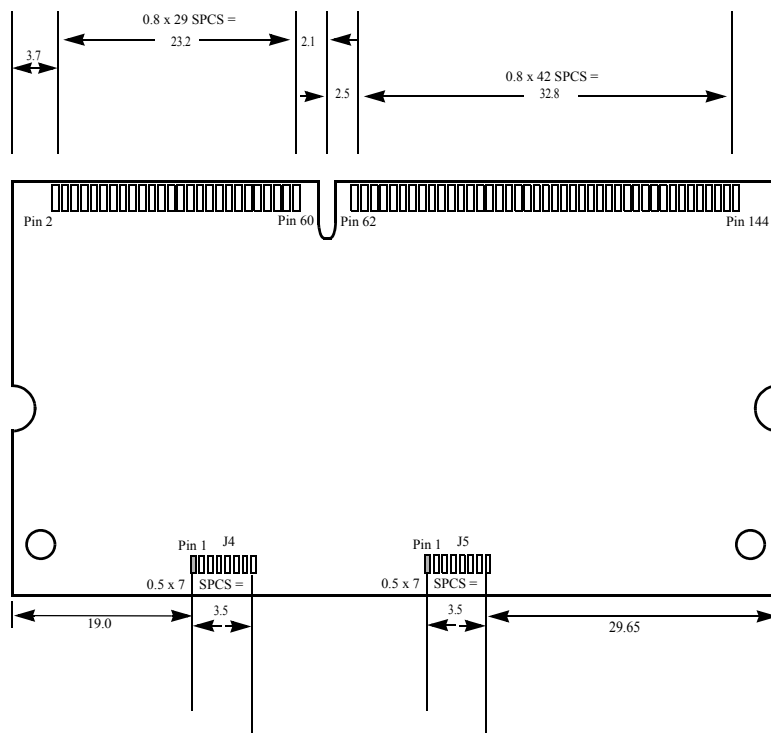


Figure 4.

Dimensions of the Trizeps-II-270M Module (bottom view)



The Maximum height is 4.0 mm above the top side and 2.0 mm below the bottom side.

Revision

Board: Trizeps-II-270M

Revision	PCB number	Date	Changes
0.1	t-ii-270-v1r111a	05.03.2010	-----