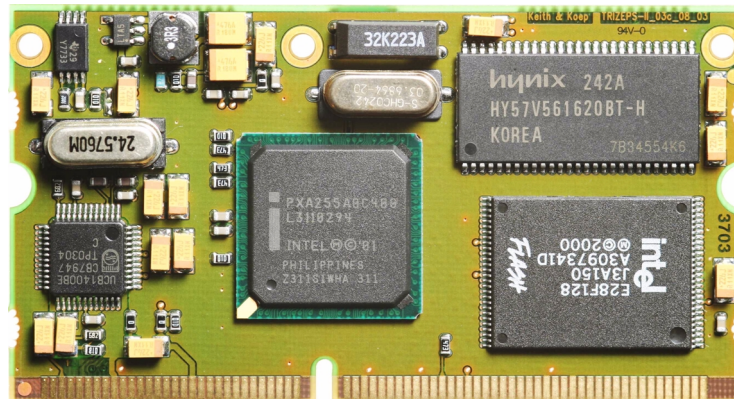


Trizeps-II-CI Module (Revision 2.1)



1.0 Introduction

The Trizeps-II Module is based on the Intel® XScale™ core-based CPU (200, 300 and 400 MHz) PXA255 - ARM¹ Architecture v.5TE compliant and application code compatible with Intel® SA-1110 processor which is used on the Trizeps-I Module. The CPU based on Intel® Superpipelined RISC technology utilizing advanced Intel 0.18μ process for high core speeds at low power (480K Dhrystone 2.1 per second @ 400 MHz). Some features of the XScale: Integrated memory and PCMCIA/CompactFlash Controller with 100MHz Memory Bus, 16-bit or 32-bit ROM/Flash/SRAM six banks, 16-bit or 32-bit SDRAM; System Control Module includes 17 dedicated general-purpose interruptible I/O ports, real-time clock, watchdog and interval timers, power management controller, interrupt and reset controller, LCD controller and two on-chip oscillators. Trizeps-II includes also the Philips UCB 1400, on a single chip it combines audio codec functions, a touch-screen controller and power management interfaces. The incorporated A/D converter and the touch screen interface provides complete control and read-out of a 4 wire resistive touch screen. Features of Trizeps-II:

Single power supply (+3V3)	-Universal serial bus device controller (UDC)
Flash memory onboard (4, 8, 16 MByte)	-Infrared communication port (ICP)
2 x synchronous DRAM (each 8, 16, 32 MByte)	-I ² C Bus
XScale PXA255	-JTAG test interface
-LCD controller for monochrome displays	UCB 1400 codec
4 Bpp to TFT 16 Bpp high resolution displays	-20-bit stereo audio codec
-3 serial interfaces - 3 UART: FFUART (Full Function UART) BTUART (Bluetooth UART) STUART (Standard UART)	-Touch screen interface
-PCMCIA interface with external buffers	-Headphone output
	-Line input
	-4 x multiplexed analog voltage inputs (10 bit ADC)

1. ARM is a trademark of ARM,Ltd.

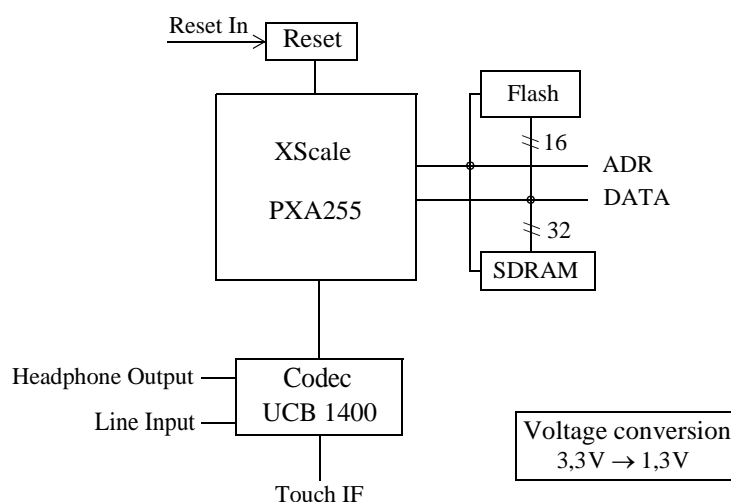
2.0 Functional description of the Trizeps-II Module

In the following you'll find special information about the Trizeps-II Module. For more information concerning the PXA255 and the UCB1400 please refer to Intel's XScale manual and Philips data sheet of the UCB 1400.

2.1 Components of the Trizeps-II Module

Figure 1.

Trizeps-II Module



Components of the Trizeps-II Module:

1. XScale PXA255 (microprocessor)
2. UCB 1400 (a single chip, stereo audio codec equipped with touch screen and power management interfaces)
3. SDRAM (synchronous DRAM)
4. Flash (Flash memory)
5. Voltage converter
6. Reset generator

2.2 Interfaces of the XScale PXA255 on SODIMM socket

The Trizeps-II Module offers the following interfaces:

2.2.1 Universal Asynchronous Receiver / Transmitter (UART) serial ports

The XScale PXA255 processor has three UARTs: Full Function UART (FFUART), Bluetooth UART (BLUART), and Standard UART (STUART).

The UARTs share the following features:

- Functionally compatible with the 16550
- Ability to add or delete standard asynchronous communications bits (start, stop and parity) in the serial data
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud rate generator that allows the internal clock to be divided by 1 to $(2^{16}-1)$ to generate an internal 16X clock
- Modem control pins that allow flow control through software

Full Function UART: All of the modem signals are accessible on the SODIMM socket.

Bluetooth UART: The signals TxD, RxD, CTS and RTS are accessible on the SODIMM socket.

Standard UART: The signals IRRxD and IRTxD are accessible on the SODIMM socket. This serial port can work as Fast Infrared Communications Port (FICP). It operates at half-duplex and provides direct connection to commercially available Infrared Data Association (IrDA) compliant LED transceivers. The FICP is based on the 4-Mbps IrDA standard and uses four-position pulse modulation (4PPM) and a specialized serial packet protocol developed for IrDA transmission. To support the standard, the FICP has:

- A bit Encoder / Decoder
- A serial-to-parallel data engine
- A transmit FIFO 128 entries deep and 8 bits wide
- A receive FIFO 128 entries deep and 11 bits wide

The FICP shares GPIO pins for transmit and receive data with the Standard UART. Only one of the ports can be used at a time.

2.2.2 Universal Serial Bus (USB) Device Controller (UDC)

The UDC supports 16 endpoints and can operate half-duplex at a rate of 12Mbps (as a slave only, not as a host or hub controller). The UDC supports four device configurations. Configurations 1, 2 and 3 each supports two interfaces. This allows the host to accommodate dynamic changes in the physical bus topology. A configuration is a specific combination of USB resources available on the device. An interface is a related set of endpoints that present a device feature or function to the host.

2.2.3 Synchronous Serial Port Controller

The Synchronous Serial Port Controller (SSPC) is a full-duplex synchronous serial interface and can connect to a variety of external analog-to-digital (A/D) converters, audio and telecom codecs, and other devices that use serial protocols for transferring data. The SSPC supports National's Microwire, Texas Instruments' Synchronous Serial Protocol (SSP), and Motorola's Serial Peripheral Interface (SPI) protocol.

The SSPC operates in master mode (the attached peripheral functions as a slave) and supports serial bit rates from 7.2 KHz to 1.84 MHz. Serial data formats may range from 4 to 16 bits in length. The SSPC provides 16 entries deep x 16 bits wide transmit and receive data FIFOs.

The FIFOs may be loaded or emptied by the Central Processor Unit (CPU) using programmed I/O, or DMA burst transfers of 4 or 8 half-words per transfer while receiving or transmitting.

2.2.4 I²C Bus Interface Unit

The I²C bus was created by the Phillips Corporation and is a serial bus with a two-pin interface. The SDA data pin is used for input and output functions and the SCL clock pin is used to control and reference the I²C bus. The I²C bus unit allows the PXA255 to serve as a master and slave device that resides on the I²C bus.

The I²C unit enables the PXA255 to communicate with I²C peripherals and micro-controllers for system management functions. The I²C bus requires a minimum amount of hardware to relay status and reliability information concerning the PXA255 subsystem to an external device.

The I²C unit is a peripheral device that resides on the PXA255 internal bus. Data is transmitted to and received from the I²C bus via a buffered interface. Control and status information is relayed through a set of memory-mapped registers. Refer to *The I²C-Bus Specification* for complete details on I²C bus operation.

2.2.5 MultiMediaCard Controller

The PXA255 MultiMediaCard (MMC) controller acts as a link between the software used to access the PXA255 and the MMC stack (a set of memory cards). The MMC controller is designed to support the MMC system, a low-cost data storage and communications system. The PXA255 MMC controller is based on the standards outlined in *The MultiMediaCard System Specification Version 2.1* with the exception that one- and three-byte data transfers are not supported and the maximum block length is 1023.

The MMC controller features:

- Data transfer rates up to 20 Mbps
- A response FIFO
- Dual receive data FIFOs
- Dual transmit data FIFOs
- Support for two MMCs in either MMC or SPI mode

2.3 Codec (UCB 1400)

Trizeps-II includes also the Philips UCB 1400. It integrates an AC '97 Rev. 2.1 interface for communication to Intel® XScale processor. If you need a detailed description please refer to Philips data sheet. For interrupt programming of the codec use GP02 (IRQ). GP02 is a general purpose input/output of the PXA255.

Features of the UCB 1400:

- Integrated AC '97 Rev. 2.1 interface.
- 20-bit stereo audio codec with programmable sample rates, input and output gain, digital sound processing, capable of driving headphones, and connecting to microphone and line level inputs.
- 4-wire resistive touch screen interface circuit supporting position, pressure and plate resistance measurements.
- 10-bit successive approximation ADC with internal track-and-hold circuit and analog multiplexer for touch screen readout and monitoring of four external high voltage (7.5 V) sources.
- Ten general purpose input/output pins.
- 3.3 V supply voltage and built-in power saving modes for portable and battery-powered applications.

2.4 Memory

The XScale PXA255 has three different memory spaces: SDRAM, Static Memory, and Card Memory.

SDRAM has four partitions, Static Memory has six, and Card space has two. When memory access attempts to burst across the boundary between adjacent partitions, ensure that the configurations for the partitions are identical. The configurations must be identical in every aspect, including external bus width and burst length.

2.4.1 SDRAM interface

The PXA255 supports the SDRAM interface, which supports four 16- and 32-bit-wide SDRAM partitions. Each partition is allocated 64 MBytes of the internal memory map, but the actual size of each partition depends on the SDRAM configuration.

The Trizeps-II uses the first ($\overline{\text{SDCS}}[0]$) of the four partition selects and 32 data-lines. Usually the memory size of SDRAM is 32 MByte, configurations with 16 or 64 MByte are also possible.

2.4.2 Static Memory interface / Variable Latency I/O interface

The static memory and variable latency I/O interface has six chip selects ($\overline{\text{CS}}[5:0]$) and 26 bits of byte address ($\text{A}[25:0]$) for access up to 64 MBytes of memory in each of six banks. Each chip select is individually programmed for selecting one of the supported static memory types:

- Non-burst ROM or Flash memory is supported on $\overline{\text{CS}}[5:0]$
- Burst ROM or Flash (with non-burst writes) is supported on $\overline{\text{CS}}[5:0]$
- Burst and non-burst SRAM is supported on $\overline{\text{CS}}[5:0]$
- Variable Latency I/O is supported on $\overline{\text{CS}}[5:0]$
- Synchronous static memory is supported on $\overline{\text{CS}}[3:0]$

The Trizeps-II Flash memory is selected by the first ($\overline{\text{CS}}[0]$) of the six chip selects and uses 16 data-lines. Usually the size of Flash memory is 16 MByte, configuration with 4 MByte is also possible.

2.4.3 16-Bit PC Card / Compact Flash Interface

The PXA255 card interface is based on *The PC Card Standard - Volume 2 - Electrical Specification, Release 2.1*, and *CF+ and CompactFlash Specification Revision 1.4*. The 16-bit PC Card / Compact Flash interface provides control signals to support any combination of 16-bit PC Card / Compact Flash for two card sockets, using address line ($\text{A}[25:0]$) and data lines ($\text{D}[15:0]$).

The PXA255 16-bit PC Card / Compact Flash Controller provides the following signals:

- $\overline{\text{PREG}}$ is muxed with $\text{A}[26]$ and selects register space (I/O or attribute) versus memory space
- $\overline{\text{POE}}$ and $\overline{\text{PWE}}$ allow memory and attributes reads and writes
- $\overline{\text{PIOR}}$, $\overline{\text{PIOW}}$ and $\overline{\text{PIOIS16}}$ control I/O reads and writes
- $\overline{\text{PWAIT}}$ allows extended access times
- $\overline{\text{PCE2}}$ and $\overline{\text{PCE1}}$ are byte select high and low for a 16-bit data bus
- $\overline{\text{PSKTSEL}}$ selects between two card sockets

2.5 Voltage converter

The Trizeps-II Module uses a single power supply of +3V3. To generate the core voltage of the PXA255 a voltage converter is used.

2.6 Reset generator

Resetting the board is possible by using the $\overline{\text{RESET_IN}}$ input or by closing the soldering bridge below the reset generator C7733.

2.7 JTAG / Debug Port

The JTAG / Debug port is essentially several shift registers, with the destination controlled by the TMS pin and data I/O with TDI / TDO. JTAG is testable via the IEEE 1149.1 (JTAG). Many use JTAG to control the address / data bus for Flash programming. $\overline{\text{TRST}}$ provides initialization of the test logic. JTAG is also a hardware debug port.

3.0 Firmware:

The Trizeps-II firmware package includes:

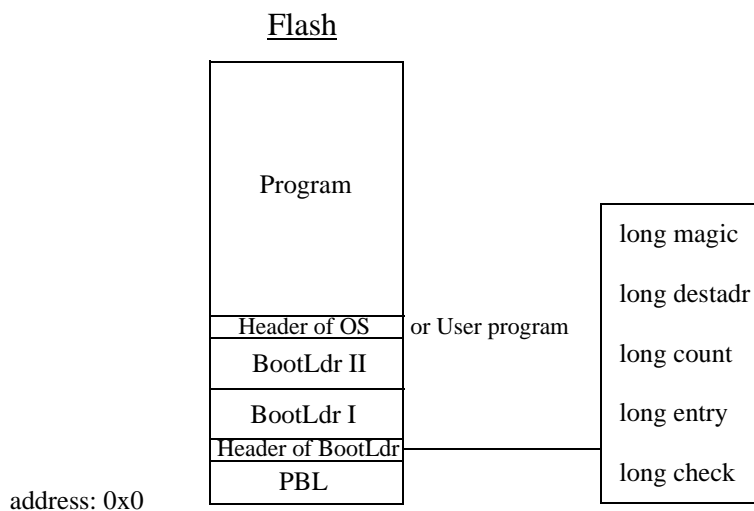
1. PBL (Primary Bootstrap Loader)
2. BOOTP/ TFTP Bootstrap Loader (Keith & Koep GmbH). It offers the following features:
 1. BOOTP/TFTP download with Ethernet support
 2. Special download with simple serial protocol
 3. Flash support
 4. On board selftest

3.1 Bootstrap procedure

After reset the processor starts the PBL (Primary Boot Loader). The PBL sets up the memory system and the MMU and decides to enter the Boot Loader or a customer program. If the soldering bridge left below SA-1110 is closed PBL will update the Boot Loader. The communication goes via RxD1, TxD1. If the bridge is open PBL looks for a valid header of a customer program (normally K&K BOOTSTRAP LOADER). If the header is valid the program will be started - otherwise the Boot Loader will be updated.

Figure 2.

Flash



If the value of magic (Flashaddress + 0x60000) is equal to 0x55aa5a5a the header is valid. The destination address (destadr) indicates the beginning of the program. Count means the length of the program. Entry indicates where to jump after loading. Check is for future use only.

4.0 DC operating conditions

1. Supply voltage 3.3 V
2. Typical operating current¹ @ 400MHz, 32MB SDRAM

Running	250 mA
Idle	120 mA
Suspend	1.8 mA

5.0 Ordering Information

1. Trizeps-II 32MB SDRAM / 16MB Flash Trizeps-II-32/16
2. Trizeps-II 64MB SDRAM / 16MB Flash Trizeps-II-64/16

1. data available in II/IV 2002

6.0 Pinout information and description

All of the significant signals are accessible via the 144-pin SODIMM socket. In addition to Trizeps module, the Trizeps-II module has an extended interface with two 32-pin contacts on the bottom side of the module. We recommend to connect the contacts with the connector with the part number 58-9158-032-000-011 by Elco

TABLE 1.

Pinout information of the connector J2 of the Trizeps-II Module (144-pin SODIMM-socket)

Pin	Name	Description
1	TSMY	Touch screen negative Y-plate (UCB 1400)
2	TSMX	Touch screen negative X-plate (UCB 1400)
3	TSPY	Touch screen positive Y-plate (UCB 1400)
4	TSPX	Touch screen positive X-plate (UCB 1400)
5	MIC_OUT	Microphone input signal (UCB 1400)
6	FF_RI / GP38	Full function UART Ring Indicator pin (PXA255)
7	MIC_GND	Microphone ground switch input (UCB 1400)
8	LINEIN_R	Line in right channel (UCB1400)
9	HEADPHONE_R	Line out right channel (UCB1400)
10	LINEIN_L	Line in left channel (UCB1400)
11	HEADPHONE_GND	Reference voltage for headphone drivers (UCB1400)
12	HEADPHONE_L	Line out left channel (UCB1400)
13	AD3	Analog voltage input (UCB 1400)
14	AD2	Analog voltage input (UCB 1400)
15	AD1	Analog voltage input (UCB 1400)
16	AD0	Analog voltage input (UCB 1400)
17	VSSA	Analog Ground (UCB1400)
18	GND	Ground
19	MMCDAT	Multimedia Card data (PXA255)
20	GP06 / MMCCLK	Multimedia Card clock(PXA255)
21	MMCCMD	Multimedia Card command(PXA255)
22	GP08 / MMCCS0	Multimedia Card chip select 0(PXA255)
23	RESET_IN	Reset input (TLC7733)
24	GP12 / MMCDET	Multimedia Card detect (PXA255)
25	RESET_OUT	Reset output (PXA255)
26	L_BIAS / GP77	LCD AC bias drive (PXA255)
27	BT_RXD / GP42	Bluetooth UART Receive pin (PXA255)
28	BATT_FAULT	Battery fault - main power is going down (PXA255)
29	BT_TXD / GP43	Bluetooth UART Transmit pin (PXA255)
30	IR_RXD / GP46	Standard UART and ICP (PXA255)
31	FF_RXD GP34	Full function UART Receive pin (PXA255)
32	IR_TXD / GP47	Standard UART and ICP (PXA255)
33	FF_TXD / GP39	Full function UART Transmit pin (PXA255)
34	TUDC-	Serial port zero bidirectional (UDC) (PXA255)

TABLE 1.

Pinout information of the connector J2 of the Trizeps-II Module (144-pin SODIMM-socket)

Pin	Name	Description
35	VDDA (+3V3)	Analog power supply (UCB 1400)
36	+3V3	Power supply
37	I2C_DATA	I ² C data (PXA255)
38	TUDC+	Serial port zero bidirectional (UDC) (PXA255)
39	SSP_TXD / GP25	Synchronous Serial Port Transmit (PXA255)
40	I2C_CLK	I ² C clock (PXA255)
41	SSPS_CLK / GP23	Synchronous Serial Port Clock (PXA255)
42	SSPS_FRM / GP24	Synchronous Serial Port Frame (PXA255)
43	DREQ0 / GP20	DMA Request (PXA255)
44	GP21	General purpose I/O (PXA255)
45	FF_DCD / GP36	Full function UART Data-Carrier-Detect pin (PXA255)
46	DREQ1 / GP19	DMA Request (PXA255)
47	FF_DTR / GP40	Full function UART Data-Terminal-Ready pin (PXA255)
48	FF_DSR / GP37	Full function UART Data-Set-Ready pin (PXA255)
49	FF_RTS / GP41	Full function UART Ready-To-Send pin (PXA255)
50	FF_CTS / GP35	Full function UART Clear-To-Send pin (PXA255)
51	BT_RTS / GP45	Bluetooth UART Ready-To-Send pin (PXA255)
52	BT_CTS / GP44	Bluetooth UART Clear-To-Send pin (PXA255)
53	GP10	General purpose I/O (PXA255)
54	GP11	General purpose I/O (PXA255)
55	LDD14 / GP72	LCD display data (PXA255)
56	LDD15 / GP73	LCD display data (PXA255)
57	LDD12 / GP70	LCD display data (PXA255)
58	LDD13 / GP71	LCD display data (PXA255)
59	LDD10 / GP68	LCD display data (PXA255)
60	LDD11 / GP69	LCD display data (PXA255)
61	LDD8 / GP66	LCD display data (PXA255)
62	LDD9 / GP67	LCD display data (PXA255)
63	GP00	General purpose I/O (PXA255)
64	GP01	General purpose I/O (PXA255)
65	GND	Ground
66	GND	Ground
67	L_FCLK / GP74	LCD frame clock (PXA255)
68	L_LCLK / GP75	LCD line clock (PXA255)
69	L_PCLK / GP76	LCD pixel clock (PXA255)
70	LDD6 / GP64	LCD display data (PXA255)
71	LDD7 / GP65	LCD display data (PXA255)
72	LDD4 / GP62	LCD display data (PXA255)
73	LDD5 / GP63	LCD display data (PXA255)

TABLE 1.

Pinout information of the connector J2 of the Trizeps-II Module (144-pin SODIMM-socket)

Pin	Name	Description
74	LDD2 / GP60	LCD display data (PXA255)
75	LDD3 / GP61	LCD display data (PXA255)
76	LDD0 / GP58	LCD display data (PXA255)
77	LDD1 / GP59	LCD display data (PXA255)
78	GND	Ground
79	$\overline{\text{PWE}}$ / GP49	PCMCIA CF write enable (PXA255)
80	$\overline{\text{POE}}$ / GP48	PCMCIA CF output enable (PXA255)
81	$\overline{\text{PIOW}}$ / GP51	PCMCIA CF I/O write (PXA255)
82	$\overline{\text{PIOR}}$ / GP50	PCMCIA CF I/O read (PXA255)
83	$\overline{\text{PWAIT}}$ / GP56	PCMCIA CF wait (PXA255)
84	$\overline{\text{PIOIS16}}$ / GP57	I/O select 16 (PXA255)
85	$\overline{\text{PREG}}$ / GP55	PCMCIA register select (PXA255)
86	PSKTSEL / GP54	PCMCIA socket select (PXA255)
87	$\overline{\text{PCE1}}$ / GP52	PCMCIA card enable 1 (low-byte lane) (PXA255)
88	$\overline{\text{PCE2}}$ / GP53	PCMCIA card enable 2 (high-byte lane) (PXA255)
89	+3V3	Power supply
90	+3V3	Power supply
91	D14	Memory data bus (PXA255)
92	D15	Memory data bus (PXA255)
93	D12	Memory data bus (PXA255)
94	D13	Memory data bus (PXA255)
95	D10	Memory data bus (PXA255)
96	D11	Memory data bus (PXA255)
97	D08	Memory data bus (PXA255)
98	D09	Memory data bus (PXA255)
99	D06	Memory data bus (PXA255)
100	D07	Memory data bus (PXA255)
101	D04	Memory data bus (PXA255)
102	D05	Memory data bus (PXA255)
103	D02	Memory data bus (PXA255)
104	D03	Memory data bus (PXA255)
105	D00	Memory data bus (PXA255)
106	D01	Memory data bus (PXA255)
107	GND	Ground
108	GND	Ground
109	RDY / GP18	Variable Latency I/O Ready pin (PXA255)
110	$\overline{\text{WE}}$	Memory write enable (PXA255)
111	$\overline{\text{RD}}/\overline{\text{WR}}$	Read/Write for static interface (PXA255)
112	$\overline{\text{OE}}$	Memory output enable (PXA255)

TABLE 1.

Pinout information of the connector J2 of the Trizeps-II Module (144-pin SODIMM-socket)

Pin	Name	Description
113	GND	Ground
114	$\overline{\text{CS5}}$ / GP33	Static chip select (PXA255)
115	$\overline{\text{CS4}}$ / GP80	Static chip select (PXA255)
116	$\overline{\text{CS3}}$ / GP79	Static chip select (PXA255)
117	$\overline{\text{CS2}}$ / GP78	Static chip select (PXA255)
118	$\overline{\text{CS1}}$ / GP15	Static chip select (PXA255)
119	A25	Memory address bus (PXA255)
120	A24	Memory address bus (PXA255)
121	A23	Memory address bus (PXA255)
122	A22	Memory address bus (PXA255)
123	A21	Memory address bus (PXA255)
124	A20	Memory address bus (PXA255)
125	A19	Memory address bus (PXA255)
126	A18	Memory address bus (PXA255)
127	A17	Memory address bus (PXA255)
128	A16	Memory address bus (PXA255)
129	A15	Memory address bus (PXA255)
130	A14	Memory address bus (PXA255)
131	A13	Memory address bus (PXA255)
132	A12	Memory address bus (PXA255)
133	A11	Memory address bus (PXA255)
134	A10	Memory address bus (PXA255)
135	A09	Memory address bus (PXA255)
136	A08	Memory address bus (PXA255)
137	A07	Memory address bus (PXA255)
138	A06	Memory address bus (PXA255)
139	A05	Memory address bus (PXA255)
140	A04	Memory address bus (PXA255)
141	A03	Memory address bus (PXA255)
142	A02	Memory address bus (PXA255)
143	A01	Memory address bus (PXA255)
144	A00	Memory address bus (PXA255)

You can get detailed information about the socket in the internet (<http://www.amp.com>). Choose search - part number and enter the number 390113-1.

TABLE 2.

Pinout information of the connector J1 of the Trizeps-II Module (32-pin contact)

Pin	Name	Description
1	GND	Ground
2	GND	Ground
3	GND	Ground
4	GND	Ground
5	-	Reserved
6	BATT_VCC	Backup battery connection (PXA255)
7	D31	Memory data bus (PXA255)
8	D16	Memory data bus (PXA255)
9	-	Reserved
10	-	Reserved
11	D30	Memory data bus (PXA255)
12	D17	Memory data bus (PXA255)
13	D29	Memory data bus (PXA255)
14	D18	Memory data bus (PXA255)
15	-	Reserved
16	-	Reserved
17	D28	Memory data bus (PXA255)
18	D19	Memory data bus (PXA255)
19	D27	Memory data bus (PXA255)
20	D20	Memory data bus (PXA255)
21	-	Reserved
22	-	Reserved
23	D26	Memory data bus (PXA255)
24	D21	Memory data bus (PXA255)
25	D25	Memory data bus (PXA255)
26	D22	Memory data bus (PXA255)
27	D24	Memory data bus (PXA255)
28	D23	Memory data bus (PXA255)
29	-	Reserved
30	$\overline{CS0}$	static chip select (PXA255)
31	GND	Ground
32	GND	Ground

TABLE 3.

Pinout information of the connector J3 of the Trizeps-II Module (32-pin contact)

Pin	Name	Description
1	GND	Ground
2	GND	Ground
3	GND	Ground
4	GND	Ground
5	DQM0	SDRAM DQM for data byte 0 (PXA255)
6	DQM1	SDRAM DQM for data byte 1 (PXA255)
7	GND	Ground
8	GND	Ground
9	DQM2	SDRAM DQM for data byte 2 (PXA255)
10	DQM3	SDRAM DQM for data byte 3 (PXA255)
11	GP14	General purpose I/O (PXA255)
12	MMCCS0 / GP08	Multimedia Card chip select 0 (PXA255)
13	MMCMD	Multimedia Card Command (PXA255)
14	MMDAT	Multimedia Card Data (PXA255)
15	PWM2	Pulse Width Modulation channel 0 (PXA255)
16	PWM1	Pulse Width Modulation channel 1 (PXA255)
17	GP13	General purpose I/O (PXA255)
18	GP07	General purpose I/O (PXA255)
19	GP12	General purpose I/O (PXA255)
20	MMCCLK / GP06	MMC clock (PXA255)
21	SSP_RXD / GP26	Synchronous Serial Port Receive (PXA255)
22	GP05	General purpose I/O (PXA255)
23	SSPEXTCLK / GP27	Synchronous Serial Port External Clock(PXA255)
24	GP04	General purpose I/O (PXA255)
25	MMCCS1 / GP09	MMC chip select 1 (PXA255)
26	GP03	General purpose I/O (PXA255)
27	+VCORE ^a	Positive supply for internal logic (PXA255)
28	GP22	General purpose I/O (PXA255)
29	+VCORE ^a	Positive supply for internal logic (PXA255)
30	+VPLL ^a	Positive supply for PLLs and oscillators (PXA255)
31	GND	Ground
32	GND	Ground

a. only for measurement

TABLE 4.

Pinout information of the connector J4 of the Trizeps-II Module (JST 08FHJ-SM1-TB, 8-pin contact)

Pin	Name	Description
1	+3V3	Power Supply
2	GND	Ground
3	TMS	JTAG test mode select (PXA255)
4	$\overline{\text{TRST}}$	JTAG test interface reset (PXA255)
5	TCK	JTAG test clock (PXA255)
6	TDO	JTAG test data output (PXA255)
7	TDI	JTAG test data input (PXA255)
8	$\overline{\text{RESET}}$	Reset input (PXA255)

Appendix

7.0 Dimensions of the Trizeps-II Module

Figure 3. Dimensions of the Trizeps-II Module (top view)

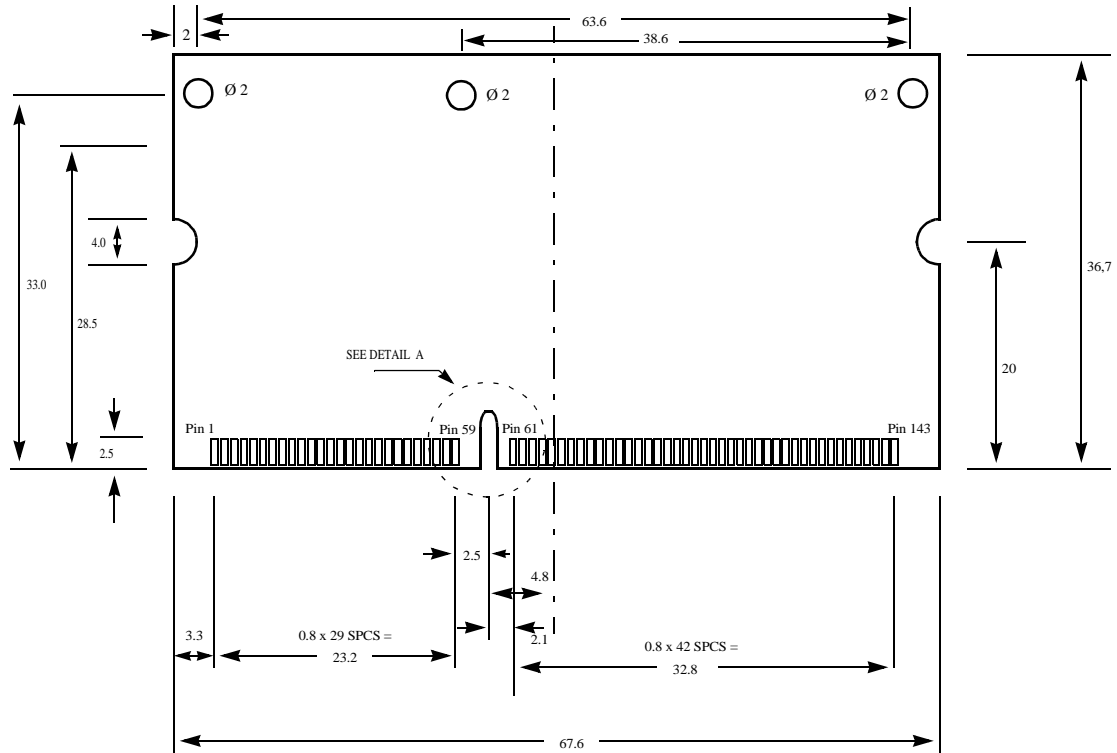


Figure 4. Detail A of Figure 3

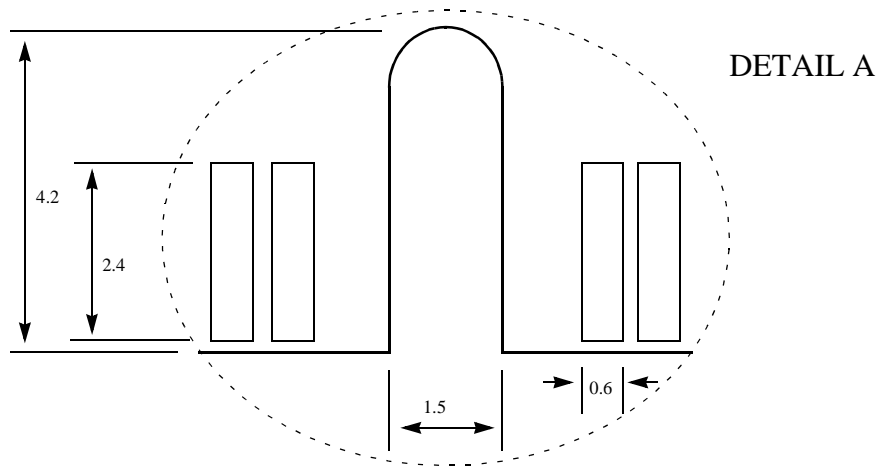
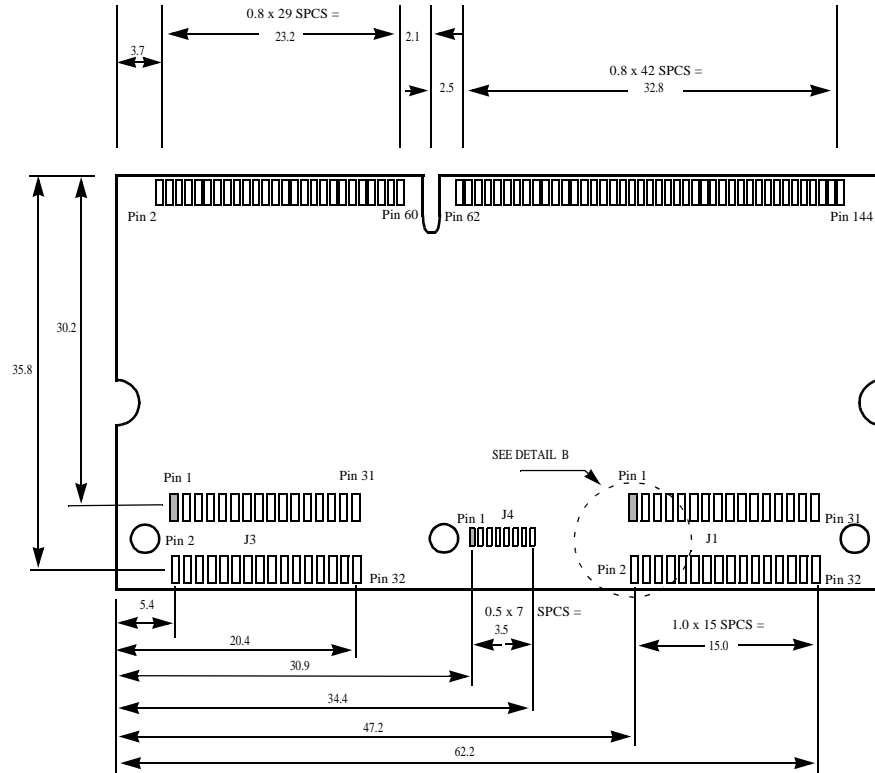
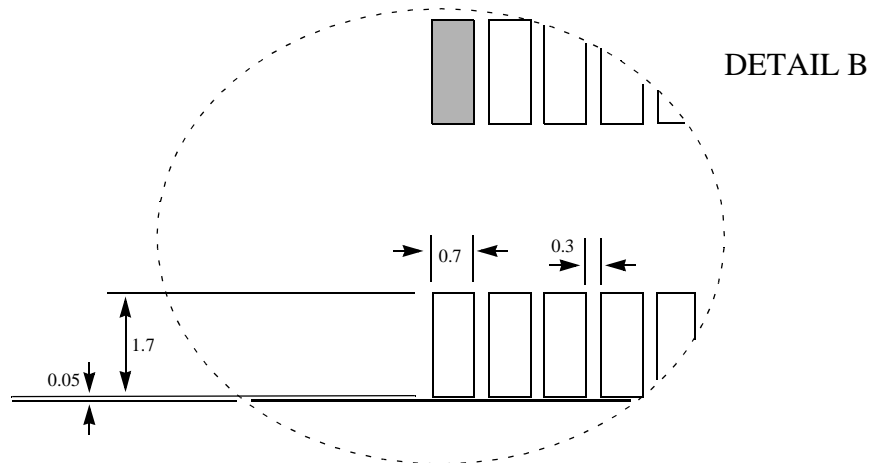


Figure 5. Dimensions of the Trizeps-II Module (bottom view)



The Maximum height is 4.0 mm above the top side and 2.0 mm below the bottom side.

Figure 6. Detail of Figure 5



Revision

Board: Trizeps-II

Revision	PCB number	Date	Changes
1.1	xx_xx_xx	03.03.02	-----
1.2	02_04_02	24.04.02	IRQ_CODEC connected to GPIO 02 GPIO 02 changed by GPIO 22 on SODIMM14-connector
1.3	dito	08.03.2003	Power-consumption added
2.0	03_05_03	14.07.2003	JTAG-signals on connector J4 Multimedia Card connection on SODIMM144-connector
2.1	dito	08.04.2004	Add definition of VDDA,VSSA (SODIMM 35,17)