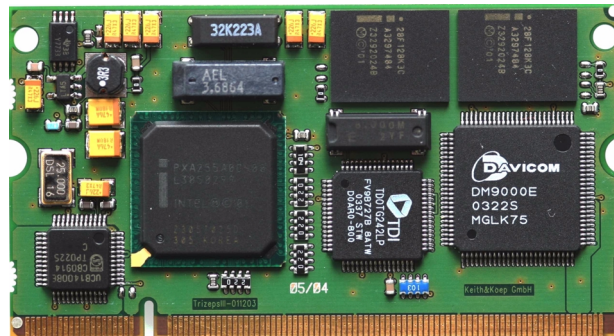


Trizeps-III Module (Preliminary)



1.0 Introduction

The Trizeps-III Module is based on the Intel® XScale™ core-based CPU (200, 300 and 400 MHz) PXA255 - ARM¹ Architecture v.5TE compliant and application code compatible with Intel® SA-1110 processor which is used on the Trizeps-I Module. The CPU based on Intel® Superpipelined RISC technology utilizing advanced Intel 0.18μ process for high core speeds at low power (670K Dhrystone 2.1 per second @ 400 MHz). Some features of the XScale: Integrated memory and PCMCIA/CompactFlash Controller with 100MHz Memory Bus, 16-bit or 32-bit ROM/Flash/SRAM six banks, 16-bit or 32-bit SDRAM; System Control Module includes 17 dedicated general-purpose interruptible I/O ports, real-time clock, watchdog and interval timers, power management controller, interrupt and reset controller, LCD controller and two on-chip oscillators. Trizeps-III includes also the Philips UCB 1400, on a single chip it combines audio codec functions, a touch-screen controller and power management interfaces. The incorporated A/D converter and the touch screen interface provides complete control and read-out of a 4 wire resistive touch screen. The additional Interfaces like USB OTG which can be driven as USB Host or Slave and the onboard 10/100MBit Ethernet Interface offer best of class integration and optimal performance together with the PXA255 embedded processor.

Features of Trizeps-III:

Single power supply (+3V3)	-Universal serial bus device controller (UDC)
2 x Flash memory onboard (each <u>16</u> or 32 MByte)	
2 x synchronous DRAM (each <u>32</u> or 64 MByte)	-Infrared communication port (ICP)
XScale PXA255	-I ² C Bus
-LCD controller for monochrome	-JTAG test interface
4 Bpp to TFT 16 Bpp high resolution displays	UCB 1400 codec
	-20-bit stereo audio codec
	-Touch screen interface

1. ARM is a trademark of ARM,Ltd.

-3 serial interfaces - 3 UART:	-Headphone output
FFUART (Full Function UART)	-Line input
BTUART (Bluetooth UART)	-4 x multiplexed analog voltage inputs
STUART (Standard UART)	(10 bit ADC)
10/100MBit Ethernet Controller	USB 2.0 OTG USB Controller
-PCMCIA interface with external buffers	

2.0 Functional description of the Trizeps-III Module

In the following you'll find special information about the Trizeps-III Module. For more information concerning the PXA255, UCB1400, OTG242 or DM9000 peripherals please refer to the manufacturers original manuals:

PXA255 <http://developer.intel.com/design/pca/applicationsprocessors/manuals>

UCB1400 <http://www.philips.com>

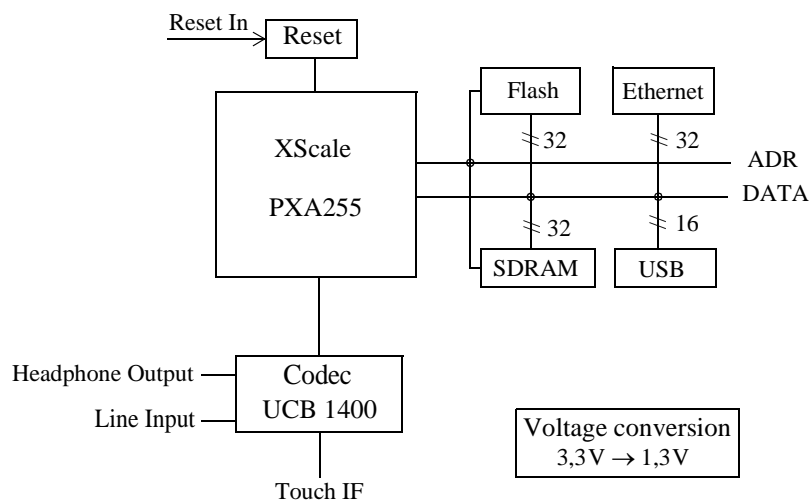
OTG242LP <http://www.transdimension.com>

DM9000 <http://davicom.co.tw>

Components of the Trizeps-III Module

Figure 1.

Trizeps-III Module



Components of the Trizeps-III Module:

1. XScale PXA255 (microprocessor)
2. UCB 1400 (a single chip, stereo audio codec equipped with touch screen and power management interfaces)
3. SDRAM (synchronous DRAM)

4. Flash (Flash memory)
5. DM9000 10/100 MBit Ethernet Controller and onboard EEPROM for mac-adr
6. OTG242 USB OTG Controller with 2 downstream and 1 upstream channels
7. Switch mode PXA255 core voltage regulator
8. Reset generator

2.1 Interfaces of the XScale PXA255 on SODIMM socket

The Trizeps-III Module offers the following interfaces:

2.1.1 Universal Asynchronous Receiver / Transmitter (UART) serial ports

The XScale PXA255 processor has four UARTs: Full Function UART (FFUART), Bluetooth UART (BLUART), and Standard UART (STUART) and Hardware UART (HWUART).

The UARTs share the following features:

- Functionally compatible with the 16550
- Ability to add or delete standard asynchronous communications bits (start, stop and parity) in the serial data
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud rate generator that allows the internal clock to be divided by 1 to $(2^{16}-1)$ to generate an internal 16X clock
- Modem control pins that allow flow control through software

Full Function UART: All of the modem signals are accessible on the SODIMM socket.

Hardware UART: Like FFUART. The HWUART controls the handshake pins automatically

Bluetooth UART: The signals TxD, RxD, CTS and RTS are accessible on the SODIMM socket.

Standard UART: The signals IRRxD and IRTxD are accessible on the SODIMM socket. This serial port can work as Fast Infrared Communications Port (FICP). It operates at half-duplex and provides direct connection to commercially available Infrared Data Association (IrDA) compliant LED transceivers. The FICP is based on the 4-Mbps IrDA standard and uses four-position pulse modulation (4PPM) and a specialized serial packet protocol developed for IrDA transmission. To support the standard, the FICP has:

- A bit Encoder / Decoder
- A serial-to-parallel data engine
- A transmit FIFO 128 entries deep and 8 bits wide
- A receive FIFO 128 entries deep and 11 bits wide

The FICP shares GPIO pins for transmit and receive data with the Standard UART. Only one of the ports can be used at a time.

2.1.2 Universal Serial Bus (USB) Device Controller (UDC)

The UDC supports 16 endpoints and can operate half-duplex at a rate of 12Mbps (as a slave only, not as a host or hub controller). The UDC supports four device configurations. Configurations 1, 2 and 3 each supports two interfaces. This allows the

host to accommodate dynamic changes in the physical bus topology. A configuration is a specific combination of USB resources available on the device. An interface is a related set of endpoints that present a device feature or function to the host.

2.1.3 Synchronous Serial Port Controller

The Synchronous Serial Port Controller (SSPC) is a full-duplex synchronous serial interface and can connect to a variety of external analog-to-digital (A/D) converters, audio and telecom codecs, and other devices that use serial protocols for transferring data. The SSPC supports National's Microwire, Texas Instruments' Synchronous Serial Protocol (SSP), and Motorola's Serial Peripheral Interface (SPI) protocol.

The SSPC operates in master mode (the attached peripheral functions as a slave) and supports serial bit rates from 7.2 KHz to 1.84 MHz. Serial data formats may range from 4 to 16 bits in length. The SSPC provides 16 entries deep x 16 bits wide transmit and receive data FIFOs.

The FIFOs may be loaded or emptied by the Central Processor Unit (CPU) using programmed I/O, or DMA burst transfers of 4 or 8 half-words per transfer while receiving or transmitting.

2.1.4 I²C Bus Interface Unit

The I²C bus was created by the Phillips Corporation and is a serial bus with a two-pin interface. The SDA data pin is used for input and output functions and the SCL clock pin is used to control and reference the I²C bus. The I²C bus unit allows the PXA255 to serve as a master and slave device that resides on the I²C bus.

The I²C unit enables the PXA255 to communicate with I²C peripherals and micro-controllers for system management functions. The I²C bus requires a minimum amount of hardware to relay status and reliability information concerning the PXA255 subsystem to an external device.

The I²C unit is a peripheral device that resides on the PXA255 internal bus. Data is transmitted to and received from the I²C bus via a buffered interface. Control and status information is relayed through a set of memory-mapped registers. Refer to *The I²C-Bus Specification* for complete details on I²C bus operation.

2.1.5 MultiMediaCard Controller

The PXA255 MultiMediaCard (MMC) controller acts as a link between the software used to access the PXA255 and the MMC stack (a set of memory cards). The MMC controller is designed to support the MMC system, a low-cost data storage and communications system. The PXA255 MMC controller is based on the standards outlined in *The MultiMediaCard System Specification Version 2.1* with the exception that one- and three-byte data transfers are not supported and the maximum block length is 1023.

The MMC controller features:

- Data transfer rates up to 20 Mbps
- A response FIFO
- Dual receive data FIFOs
- Dual transmit data FIFOs
- Support for two MMCs in either MMC or SPI mode

2.2 Codec (UCB 1400)

Trizeps-III includes also the Philips UCB 1400. It integrates an AC '97 Rev. 2.1 interface for communication to Intel® XScale processor. If you need a detailed description please refer to Philips data sheet. For interrupt programming of the codec use GP02 (IRQ). GP02 is a general purpose input/output of the PXA255.

Features of the UCB 1400:

- Integrated AC '97 Rev. 2.1 interface.
- 20-bit stereo audio codec with programmable sample rates, input and output gain, digital sound processing, capable of driving headphones, and connecting to microphone and line level inputs.
- 4-wire resistive touch screen interface circuit supporting position, pressure and plate resistance measurements.
- 10-bit successive approximation ADC with internal track-and-hold circuit and analog multiplexer for touch screen readout and monitoring of four external high voltage (7.5 V) sources.
- Ten general purpose input/output pins.
- 3.3 V supply voltage and built-in power saving modes for portable and battery-powered applications.

2.3 Memory

The XScale PXA255 has three different memory spaces: SDRAM, Static Memory, and Card Memory.

SDRAM has four partitions, Static Memory has six, and Card space has two. When memory access attempts to burst across the boundary between adjacent partitions, ensure that the configurations for the partitions are identical. The configurations must be identical in every aspect, including external bus width and burst length.

2.3.1 SDRAM interface

The PXA255 supports the SDRAM interface, which supports four 16- and 32-bit-wide SDRAM partitions. Each partition is allocated 64 MBytes of the internal memory map, but the actual size of each partition depends on the SDRAM configuration.

The Trizeps-III uses the first ($\overline{\text{SDCS}}[0]$) of the four partition selects and 32 data-lines. Usually the memory size of SDRAM is 64 MByte, configuration with 128 MByte is also possible. The 128 MByte Version uses $\overline{\text{SDCS}}[0,1]$ as it needs the range of 2 address spaces. An external logic maps those lines to different banks of the SDRAMs.

2.3.2 Static Memory interface / Variable Latency I/O interface

The static memory and variable latency I/O interface has six chip selects ($\overline{\text{CS}}[5:0]$) and 26 bits of byte address ($A[25:0]$) for access up to 64 MBytes of memory in each of six banks. Each chip select is individually programmed for selecting one of the supported static memory types:

- Non-burst ROM or Flash memory is supported on $\overline{\text{CS}}[5:0]$
- Burst ROM or Flash (with non-burst writes) is supported on $\overline{\text{CS}}[5:0]$
- Burst and non-burst SRAM is supported on $\overline{\text{CS}}[5:0]$
- Variable Latency I/O is supported on $\overline{\text{CS}}[5:0]$

- Synchronous static memory is supported on $\overline{\text{CS}}[3:0]$
The Trizeps-III Flash memory is selected by the first ($\overline{\text{CS}}[0]$) of the six chip selects and uses 32 data-lines. Usually the size of Flash memory is 32 MByte, configuration with 64 MByte is also possible.

2.3.3 16-Bit PC Card / Compact Flash Interface

The PXA255 card interface is based on *The PC Card Standard - Volume 2 - Electrical Specification, Release 2.1*, and *CF+ and CompactFlash Specification Revision 1.4*. The 16-bit PC Card / Compact Flash interface provides control signals to support any combination of 16-bit PC Card / Compact Flash for two card sockets, using address line (A[25:0]) and data lines (D[15:0]).

The PXA255 16-bit PC Card / Compact Flash Controller provides the following signals:

- $\overline{\text{PREG}}$ is muxed with A[26] and selects register space (I/O or attribute) versus memory space
- $\overline{\text{POE}}$ and $\overline{\text{PWE}}$ allow memory and attributes reads and writes
- $\overline{\text{PIOR}}$, $\overline{\text{PIOW}}$ and $\overline{\text{PIOIS16}}$ control I/O reads and writes
- $\overline{\text{PWAIT}}$ allows extended access times
- $\overline{\text{PCE2}}$ and $\overline{\text{PCE1}}$ are byte select high and low for a 16-bit data bus
- PSKTSEL selects between two card sockets

2.4 Ethernet Controller (nCS2, GPIO19, 32Bit VLIO)

The TrizepsIII Module contains a high performance ethernet controller from Davicom. The MAC Address is stored into an on board EEPROM. The chip select is given by nCS2 and the interrupt is made by GPIO19. All 32 datalines are used to use the available bandwidth.

2.5 OTG242 USB Host/Slave (nCS5, GPIO5, 16Bit)

The board features Transdimension's high performance embedded USB host/slave controller. This controller is capable of the USB 2.0 OTG protocol and has a maximal bitrate of 12 Mbps. The chip is optimized to generate minimum CPU overhead.

2.6 Voltage converter

The Trizeps-III Module uses a single power supply of +3V3. To generate the core voltage of the PXA255 a high efficiency switch-mode voltage converter is used.

2.7 Reset generator

Resetting the board is possible by using the $\overline{\text{RESET_IN}}$ input or by closing the soldering bridge close to the reset generator C7733.

2.8 JTAG / Debug Port

The JTAG / Debug port consists of several shift registers, with the destination controlled by the TMS pin and data I/O with TDI / TDO. The JTAG / Debug port provides two different functionalities:

- Programming Flash memory by pushing data through the shift registers
- Hardware-testing using boundary scan interface according to IEEE 1149.1

3.0 Firmware:

The Trizeps-III firmware package includes:

1. PBL (Primary Bootstrap Loader)
2. BOOTP/ TFTP Bootstrap Loader (Keith & Koep GmbH). It offers the following features:
 1. BOOTP/TFTP download with Ethernet support
 2. Special download with simple serial protocol
 3. Flash support
 4. On board selftest
 5. SD/MMC Support (including FAT)

3.1 Bootstrap procedure

After reset the processor starts the PBL (Primary Boot Loader). The PBL sets up the memory system and the MMU and decides to enter the Boot Loader or a customer program. The communication goes via RxD1, TxD1. You can find more information about booting using the document „bootloader.pdf“.

4.0 DC operating conditions

1. Supply voltage 3.3 V
2. Typical operating current @400MHz, 32MB SDRAM
 - Running 250 mA (No Ethernet,USB)
 - Idle 120 mA (No Ethernet,USB)
 - Suspend 1.8 mA (No Ethernet,USB)

5.0 Ordering Information

1. Trizeps-III 64MB SDRAM / 32MB Flash Trizeps-III-64/32
2. Trizeps-III 128MB SDRAM / 32MB Flash Trizeps-III-128/32

6.0 Pinout information and description

All of the significant signals are accessible via the 200-pin SODIMM socket.

TABLE 1.

Pinout information of the connector J2 of the Trizeps-III Module (200-pin SODIMM-socket)

Pin	Name	Description
1	MIC_OUT	microphone input signal (UCB 1400)
2	AD3	analog voltage input (UCB 1400)
3	MIC_GND	microphone ground switch input (UCB 1400)
4	VIN_AD2	analog voltage input (UCB 1400)
5	LINEIN_L	Line in left channel (UCB1400)
6	AD1	analog voltage input (UCB 1400)
7	LINEIN_R	Line in right channel (UCB1400)
8	VBAT_AD0	analog voltage input (UCB 1400)
9	VSSA_AUDIO	Analog ground audio (UCB 1400)
10	VDDA_AUDIO	Analog power audio (UCB 1400)
11	VSSA_AUDIO	Analog ground audio (UCB 1400)
12	VDDA_AUDIO	Analog power audio (UCB 1400)
13	HEADPHONE_GND	Line out ground output (UCB 1400)
14	TSPX	positive X-plate touch screen (UCB 1400)
15	HEADPHONE_L	Line out left channel (UCB1400)
16	TSMX	negative X-plate touch screen (UCB 1400)
17	HEAPHONE_R	Line out right channel (UCB 1400)
18	TSPY	positive Y-plate touch screen (UCB 1400)
19	RXD_2	serial port two receive pin (IrDA) (PXA 255)
20	TSMY	negative Y-plate touch screen (UCB 1400)
21	TXD_2	serial port two transmit pin (IrDA) (PXA 255)
22	VDD_FAULT	Main power source goes out of regulation (PXA 255)
23	FF_DTR	Full Function UART Data Terminal Ready (PXA 255)
24	BATT_FAULT	Main battery is low or removed (PXA 255)
25	FF_CTS	Full Function UART Clear To Send (PXA 255)
26	$\overline{\text{RESET_IN}}$	reset input
27	FF_RTS	Full Function UART Ready To Send (PXA 255)
28	TUDC-	serial port zero bidirectional (UDC) (PXA 255)
29	FF_DSR	Full Function UART Data Set Ready (PXA 255)
30	TUDC+	serial port zero bidirectional (UDC) (PXA 255)
31	FF_DCD	Full Function UART Data Carrier Detect (PXA 255)
32	BT_CTS	BlueTooth UART Clear To Send (PXA 255)
33	FF_RXD	Full Function UART Receive Data (PXA 255)
34	BT_RTS	BlueTooth UART Ready To Send (PXA 255)
35	FF_TXD	Full Function UART Transmit Data (PXA 255)
36	BT_RXD	BlueTooth UART Receive Data (PXA 255)

TABLE 1.

Pinout information of the connector J2 of the Trizeps-III Module (200-pin SODIMM-socket)

Pin	Name	Description
37	FF_RI	Full Function UART Ring Indicator (PXA 255)
38	BT_TXD	BlueTooth UART Transmit Data (PXA 255)
39	GND	Ground
40	+3V3	Power Supply
41	GND	Ground
42	+3V3	Power Supply
43	GPIO00_IRQ_PIC	General purpose I/O (PXA 255)
44	L_BIAS	LCD controller display data (PXA 255)
45	GPIO01_PRDY	General purpose I/O (PXA 255)
46	LDD07	LCD controller display data (PXA 255)
47	GPIO06_MMC_CLK	General purpose I/O (PXA 255)
48	LDD09	LCD controller display data (PXA 255)
49	GPIO07	General purpose I/O (PXA 255)
50	LDD11	LCD controller display data (PXA 255)
51	GPIO08_MMC_CS0	General purpose I/O (PXA 255)
52	LDD12	LCD controller display data (PXA 255)
53	GPIO09	General purpose I/O (PXA 255)
54	LDD13	LCD controller display data (PXA 255)
55	GPIO10_IRQ_USB_SL	General purpose I/O (PXA 255)
56	L_PCLK	LCD pixel clock (PXA 255)
57	GPIO11	General purpose I/O (PXA 255)
58	LDD03	LCD controller display data (PXA 255)
59	GPIO12_MMC_DET	General purpose I/O (PXA 255)
60	LDD02	LCD controller display data (PXA 255)
61	GPIO13	General purpose I/O (PXA 255)
62	LDD08	LCD controller display data (PXA 255)
63	GPIO14	General purpose I/O (PXA 255)
64	LDD15	LCD controller display data (PXA 255)
65	GPIO16	General purpose I/O (PXA 255)
66	LDD14	LCD controller display data (PXA 255)
67	GPIO17	General purpose I/O (PXA 255)
68	L_LCLK	LCD line clock (PXA 255)
69	GPIO20/ $\overline{\text{IRQ_HIL}}$	General purpose I/O (PXA 255)
70	LDD01	LCD controller display data (PXA 255)
71	GPIO21_TTLIO_IRQ	General purpose I/O (PXA 255)
72	LDD05	LCD controller display data (PXA 255)
73	GPIO32	General purpose I/O (PXA 255)
74	LDD10	LCD controller display data (PXA 255)
75	GPIO23	General purpose I/O (PXA 255)

TABLE 1.

Pinout information of the connector J2 of the Trizeps-III Module (200-pin SODIMM-socket)

Pin	Name	Description
76	LDD00	LCD controller display data (PXA 255)
77	GPIO24_PCD	General purpose I/O (PXA 255)
78	LDD04	LCD controller display data (PXA 255)
79	GPIO25_POWERFAIL	General purpose I/O (PXA 255)
80	LDD06	LCD controller display data (PXA 255)
81	GPIO26	General purpose I/O (PXA 255)
82	L_FCLK	LCD frame clock (PXA 255)
83	GND	Ground
84	+3V3	Power Supply
85	GPIO27_RESET_BT	General purpose I/O (PXA 255)
86	NSSPFRM	Network Synchronous Serial port frame (PXA 255)
87	RESET_OUT	Reset output (PXA 255)
88	NSSPCLK	Network Synchronous Serial port clock (PXA 255)
89	WE	Memory Write Enable (PXA 255)
90	NSSPRXD	Network Synchronous Serial port receive (PXA 255)
91	OE	Memory Output Enable (PXA 255)
92	NSSPTXD	Network Synchronous Serial port transmit (PXA 255)
93	RD/WR	read/write direction control for memory bus (PXA255)
94	PCE1	PCMCIA card enable (low-byte lane) (PXA 255)
95	GPIO18/RDY	General purpose I/O (PXA 255)
96	PCE2	PCMCIA card enable (high-byte lane) (PXA 255)
97	POE	PCMCIA output enable (PXA 255)
98	PREG	PCMCIA register select (PXA 255)
99	PWE	PCMCIA write enable (PXA 255)
100	PSKTSEL	PCMCIA socket select (PXA 255)
101	PIOW	PCMCIA I/O write (PXA 255)
102	PWAIT	PCMCIA wait (PXA 255)
103	PIOR	PCMCIA I/O read (PXA 255)
104	PIOIS16	I/O select 16 (PXA 255)
105	CS1	static chip select (PXA 255)
106	CS4	static chip select (PXA 255)
107	CS3	static chip select (PXA 255)
108	+3V3	Power Supply
109	GND	Ground
110	A08	memory address bus (PXA 255)
111	A00	memory address bus (PXA 255)
112	A09	memory address bus (PXA 255)
113	A01	memory address bus (PXA 255)

TABLE 1.

Pinout information of the connector J2 of the Trizeps-III Module (200-pin SODIMM-socket)

Pin	Name	Description
114	A10	memory address bus (PXA 255)
115	A02	memory address bus (PXA 255)
116	A11	memory address bus (PXA 255)
117	A03	memory address bus (PXA 255)
118	A12	memory address bus (PXA 255)
119	A04	memory address bus (PXA 255)
120	A13	memory address bus (PXA 255)
121	A05	memory address bus (PXA 255)
122	A14	memory address bus (PXA 255)
123	A06	memory address bus (PXA 255)
124	A15	memory address bus (PXA 255)
125	A07	memory address bus (PXA 255)
126	DQM0	SDRAM DQM for data byte 0 (PXA 255)
127	$\overline{\text{OTG_EXTVB0}}$	Turn on/off the external Vbus for OTG operation (OTG 242)
128	DQM1	SDRAM DQM for data byte 1 (PXA 255)
129	$\overline{\text{OTG_PO}}$	Turn on/off the gang power for all host ports (OTG 242)
130	DQM2	SDRAM DQM for data byte 2 (PXA 255)
131	$\overline{\text{OTG_OC}}$	Over current condition indicator for gang powered host ports (OTG 242)
132	DQM3	SDRAM DQM for data byte 3 (PXA 255)
133	OTG_VBP	Vbus pulsing control (OTG 242)
134	A25	memory address bus (PXA 255)
135	OTG_VBUS	Vbus input sampled during HNP/SRP operations by the OTG port (OTG 242)
136	A24	memory address bus (PXA 255)
137	OTG_ID	Connected to the ID pin of the Mini-AB connector for OTG applications (OTG 242)
138	A23	memory address bus (PXA 255)
139	OTG_DP2	Data line for port 2 (OTG 242)
140	A22	memory address bus (PXA 255)
141	OTG_DM2	Data line for port 2 (OTG 242)
142	A21	memory address bus (PXA 255)
143	OTG_DP1	Data line for port 1 (OTG 242)
144	A20	memory address bus (PXA 255)
145	OTG_DM1	Data line for port 1 (OTG 242)
146	A19	memory address bus (PXA 255)
147	GND	Ground
148	+3V3	Power Supply

TABLE 1.

Pinout information of the connector J2 of the Trizeps-III Module (200-pin SODIMM-socket)

Pin	Name	Description
149	D00	memory data (PXA 255)
150	D16	memory data (PXA 255)
151	D01	memory data (PXA 255)
152	D17	memory data (PXA 255)
153	D02	memory data (PXA 255)
154	D18	memory data (PXA 255)
155	D03	memory data (PXA 255)
156	D19	memory data (PXA 255)
157	D04	memory data (PXA 255)
158	D20	memory data (PXA 255)
159	D05	memory data (PXA 255)
160	D21	memory data (PXA 255)
161	D06	memory data (PXA 255)
162	D22	memory data (PXA 255)
163	D07	memory data (PXA 255)
164	D23	memory data (PXA 255)
165	D08	memory data (PXA 255)
166	D24	memory data (PXA 255)
167	D09	memory data (PXA 255)
168	D25	memory data (PXA 255)
169	D10	memory data (PXA 255)
170	D26	memory data (PXA 255)
171	D11	memory data (PXA 255)
172	D27	memory data (PXA 255)
173	D12	memory data (PXA 255)
174	D28	memory data (PXA 255)
175	D13	memory data (PXA 255)
176	D29	memory data (PXA 255)
177	D14	memory data (PXA 255)
178	D30	memory data (PXA 255)
179	D15	memory data (PXA 255)
180	D31	memory data (PXA 255)
181	GND	Ground
182	+3V3	Power Supply
183	$\overline{\text{ETH_LINK_AKT}}$	Link LED signal (DM 9000)
184	A18	memory address bus (PXA 255)
185	$\overline{\text{ETH_SPEED100}}$	Speed LED signal (DM 9000)
186	A17	memory address bus (PXA 255)
187	ETH_TX0-	TP TX Output (DM 9000)

TABLE 1.

Pinout information of the connector J2 of the Trizeps-III Module (200-pin SODIMM-socket)

Pin	Name	Description
188	A16	memory adress bus (PXA 255)
189	ETH_TX0+	TP TX Output (DM 9000)
190	MMC_CMD	MultiMedia Card Command (PXA 255)
191	ETH_AGND	Analog Ground (DM 9000)
192	MMC_DAT	MultiMedia Card Data (PXA 255)
193	ETH_RXI-	TP RX Input (DM 9000)
194	I2C_DATA	I ² C data (PXA 255)
195	ETH_RXI+	TP RX Input (DM 9000)
196	I2C_CLK/ANGBOOT	I ² C data (PXA 255)
197	GND	Ground
198	+3V3	Power Supply
199	GND	Ground
200	+3V3	Power Supply

We recommended the 200-pin SODIMM connector by Tyco Electronics with the part number 1376408-1

TABLE 2.

Pinout information of the connector J4 of the Trizeps-III Module (JST 08FHJ-SM1-TB, 8-pin contact)

Pin	Name	Description
1	+3V3	Power Supply
2	GND	Ground
3	TMS	JTAG test mode select (PXA255)
4	$\overline{\text{TRST}}$	JTAG test interface reset (PXA255)
5	TCK	JTAG test clock (PXA255)
6	TDO	JTAG test data output (PXA255)
7	TDI	JTAG test data input (PXA255)
8	$\overline{\text{RESET}}$	Reset input (PXA255)

Appendix

7.0 Dimensions of the Trizeps-III Module

Figure 2. Dimensions of the Trizeps-III Module (top view)

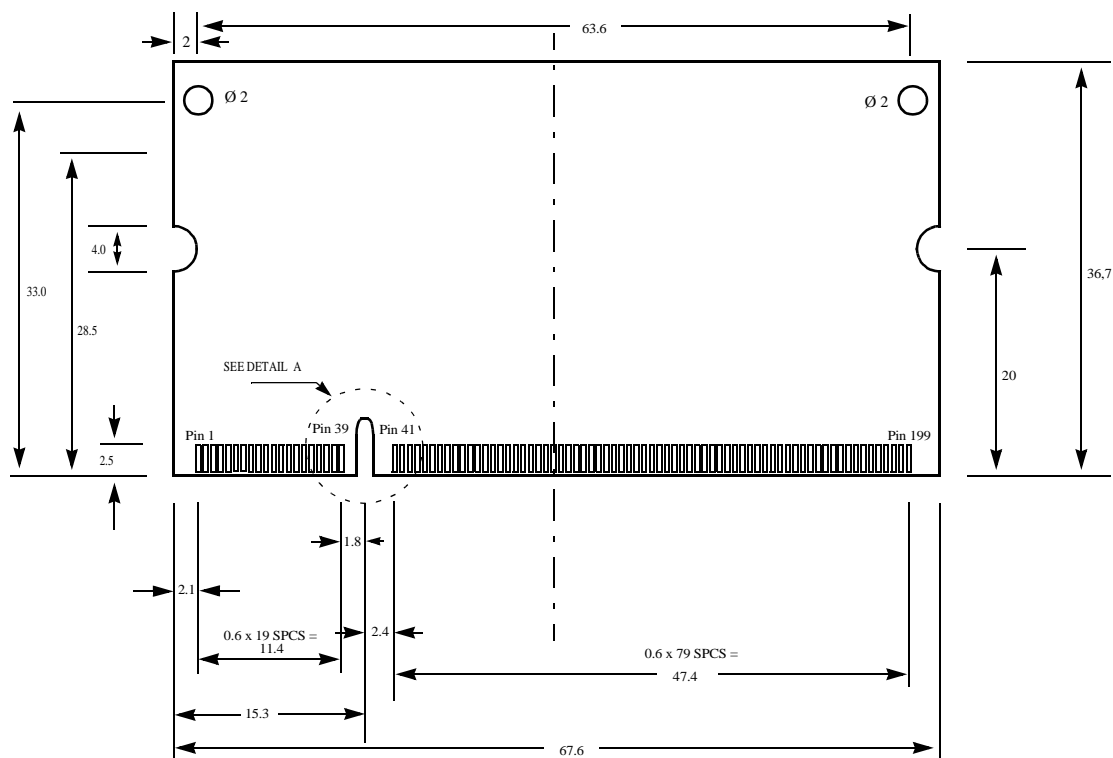


Figure 3. Detail A of Figure 3

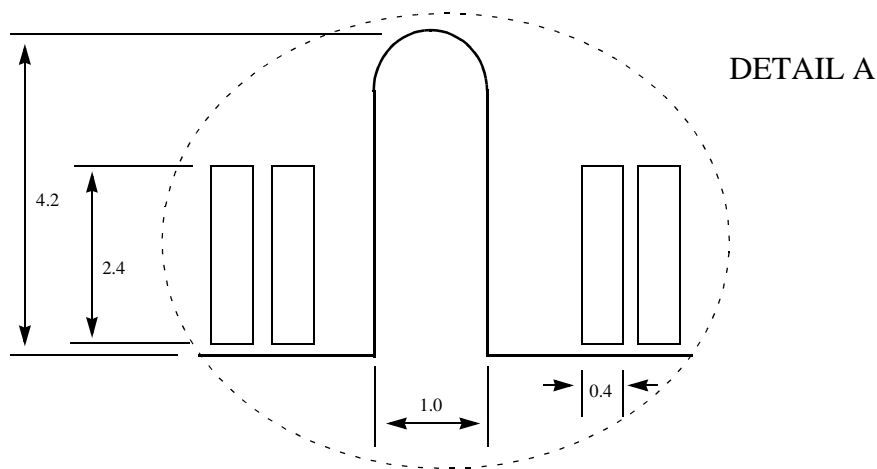
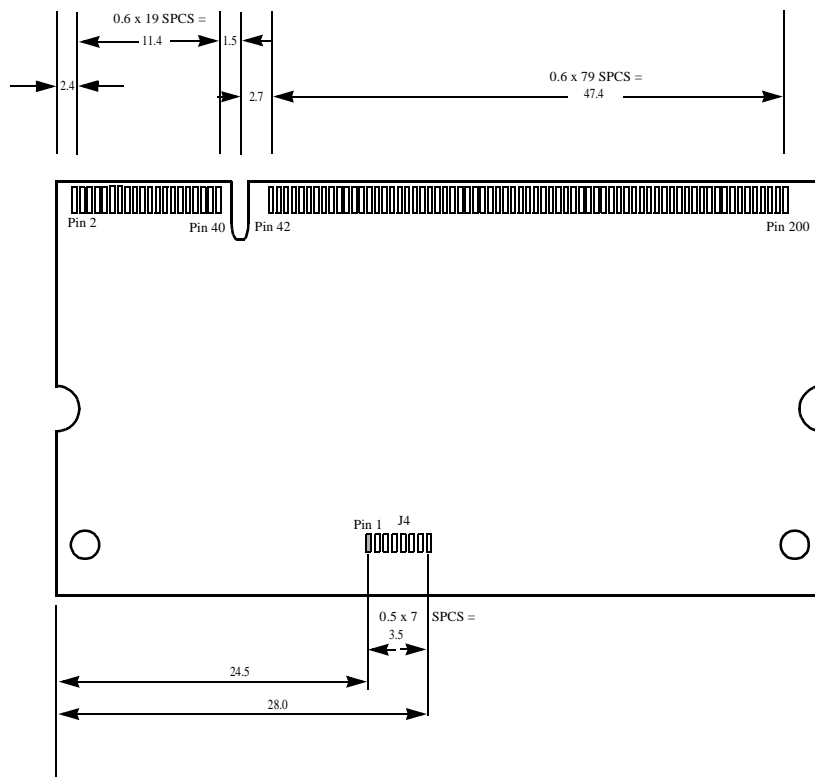


Figure 4.

Dimensions of the Trizeps-III Module (bottom view)



The Maximum height is 4.0 mm above the top side and 2.0 mm below the bottom side.

Revision

Board: Trizeps-III

Revision	PCB number	Date	Changes
1.1	011203	03.03.04	Initial Version
1.2	011203	30.07.04	minor doc changes
1.3	011203	02.09.04	minor doc changes